harman kardon
Model DVD 27

DVD/CD/CD-R/CD-RW/VCD MP3 Player

Service Manual



- Contents -

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Rev0 3/2006

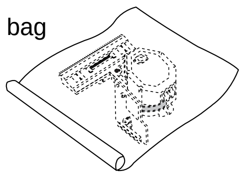
SERVICING PRECAUTIONS

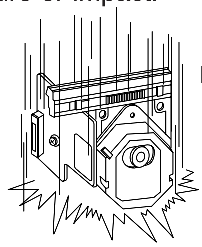
NOTES REGARDING HANDLING OF THE PICK-UP

1. Notes for transport and storage

1) The pick-up should always be left in its conductive bag until immediately prior to use.
2) The pick-up should never be subjected to external pressure or impact.

Storage in conductive bag

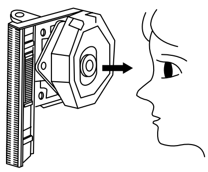




Drop impact

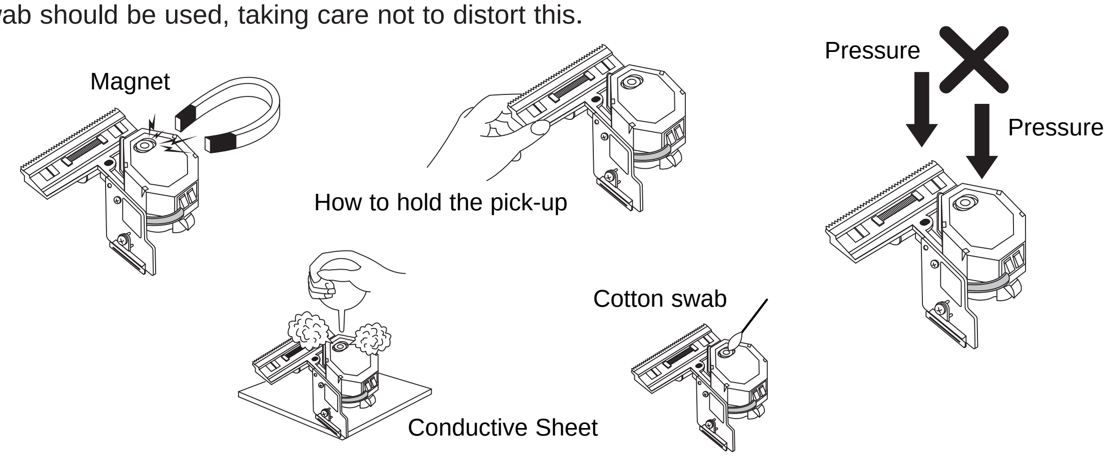
2. Repair notes

1) The pick-up incorporates a strong magnet, and so should never be brought close to magnetic materials.
2) The pick-up should always be handled correctly and carefully, taking care to avoid external pressure and impact. If it is subjected to strong pressure or impact, the result may be an operational malfunction and/or damage to the printed-circuit board.
3) Each and every pick-up is already individually adjusted to a high degree of precision, and for that reason the adjustment point and installation
   screws should absolutely never be touched.
4) Laser beams may damage the eyes!
   Absolutely never permit laser beams to enter the eyes!
   Also NEVER switch ON the power to the laser output part (lens, etc.) of the pick-up if it is damaged.



NEVER look directly at the laser beam, and don't let contact fingers or other exposed skin.

5) Cleaning the lens surface
   If there is dust on the lens surface, the dust should be cleaned away by using an air bush (such as used for camera lens). The lens is held by a delicate spring. When cleaning the lens surface, therefore, a cotton swab should be used, taking care not to distort this.



6) Never attempt to disassemble the pick-up.
   Spring by excess pressure. If the lens is extremely dirty, apply isopropyl alcohol to the cotton swab. (Do not use any other liquid cleaners, because they will damage the lens.) Take care not to use too much of this alcohol on the swab, and do not allow the alcohol to get inside the pick-up.

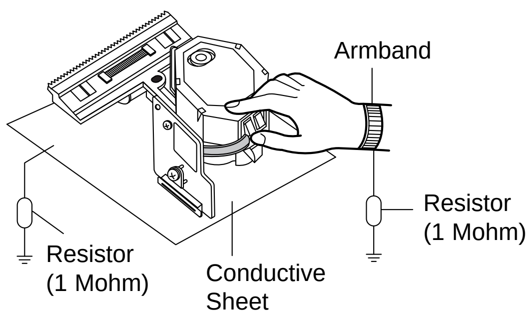
NOTES REGARDING COMPACT DISC PLAYER REPAIRS

1. Preparations

1) Compact disc players incorporate a great many ICs as well as the pick-up (laser diode). These components are sensitive to, and easily affected by, static electricity. If such static electricity is high voltage, components can be damaged, and for that reason components should be handled with care.
2) The pick-up is composed of many optical components and other high-precision components. Care must be taken, therefore, to avoid repair or storage where the temperature of humidity is high, where strong magnetism is present, or where there is excessive dust.

2. Notes for repair

1) Before replacing a component part, first disconnect the power supply lead wire from the unit
2) All equipment, measuring instruments and tools must be grounded.
3) The workbench should be covered with a conductive sheet and grounded.
   When removing the laser pick-up from its conductive bag, do not place the pick-up on the bag. (This is because there is the possibility of damage by static electricity.)
4) To prevent AC leakage, the metal part of the soldering iron should be grounded.
5) Workers should be grounded by an armband (1MΩ)
6) Care should be taken not to permit the laser pick-up to come in contact with clothing, in order to prevent static electricity changes in the clothing to escape from the armband.
7) The laser beam from the pick-up should NEVER be directly facing the eyes or bare skin.



ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will by installed.

CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

DVD 27 TECHNICAL SPECIFICATIONS

Applicable Disc:	Disc formats: 5-inch (12cm) or 3-inch (8cm) DVD-Video, Standard conforming DVD-R, DVD+R, DVD-RW, DVD+RW, VCD, CD, CD-R, CD-RW or MP3 discs Region code: DVD Video disc with Code 1 or 0 only DVD-Layers: Single Side/Single Layer, Single Side/Dual Layer, Dual Side/Dual Layer Audio formats: Linear PCM, MPEG, Windows Media 8, Dolby Digital or DTS Audio Discs Still image format: JPEG
Video Signal System:	NTSC
Composite Video Output:	1V p-p/75 ohms, sync negative polarity
S-Video Output:	Y/Luminance: 1V p-p/75 ohms, sync negative polarity C/Chrominance: 0.286V p-p
Component Video Output:	Y: 1V p-p/75 ohms, sync negative polarity Pr: 0.7V p-p/75 ohms Pb: 0.7V p-p/75 ohms
Analog Audio Output:	2V rms (1kHz, 0dB)
Frequency Response:	DVD (Linear PCM): 2Hz – 22kHz +0/–0.5dB (48kHz sampling) 2Hz – 44kHz +0/–1.5dB (96kHz sampling) CD: 2Hz – 20kHz +0/–0.5dB
Signal/Noise Ratio (SNR):	105dB (A-weighted)
Dynamic Range:	DVD: 100dB (18-bit)/105dB (20-bit) CD/DVD: 96dB (16-bit)
THD/1kHz:	DVD/CD: 0.0025%
Wow & Flutter:	Below Measurable Limits
AC Power:	110–240VAC/50–60Hz
Power Consumption:	1 Watt (On/Standby)/11 Watts (Max)
Dimensions (H x W x D):	17-3/10" x 1-15/16" x 12" (440mm x 49mm x 330mm) 2" x 17-3/10" x 11-1/4" (50mm x 440mm x 285mm)
Weight:	6 lb (2.7kg)
Shipping Dimensions (H x W x D):	5" x 14-3/8" x 20" (127mm x 365mmx 508mm)
Shipping Weight:	8.8 lb (4kg)

Depth measurement includes knobs and connectors.

Height measurement includes feet and chassis.

All specifications subject to change without notice.

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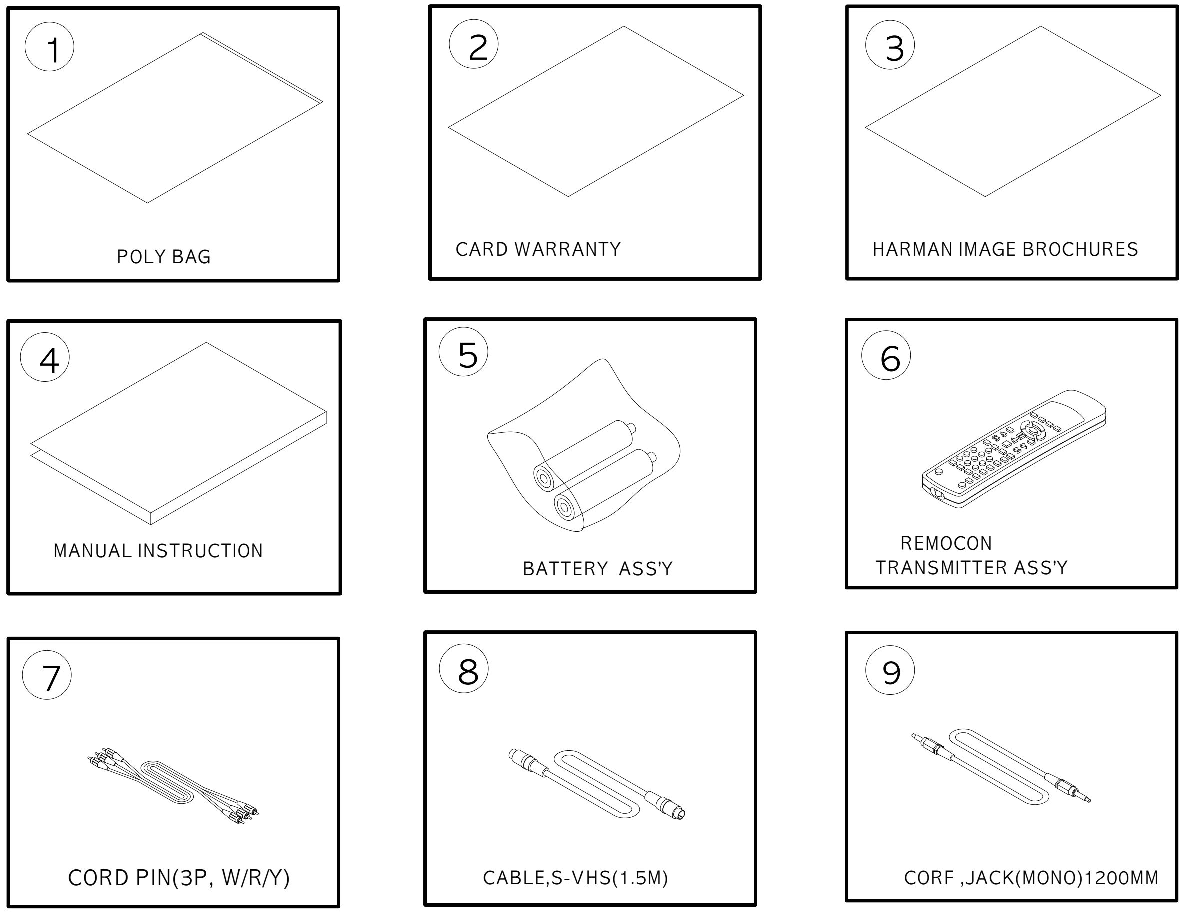
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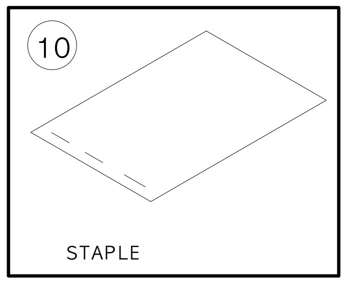
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DVD27

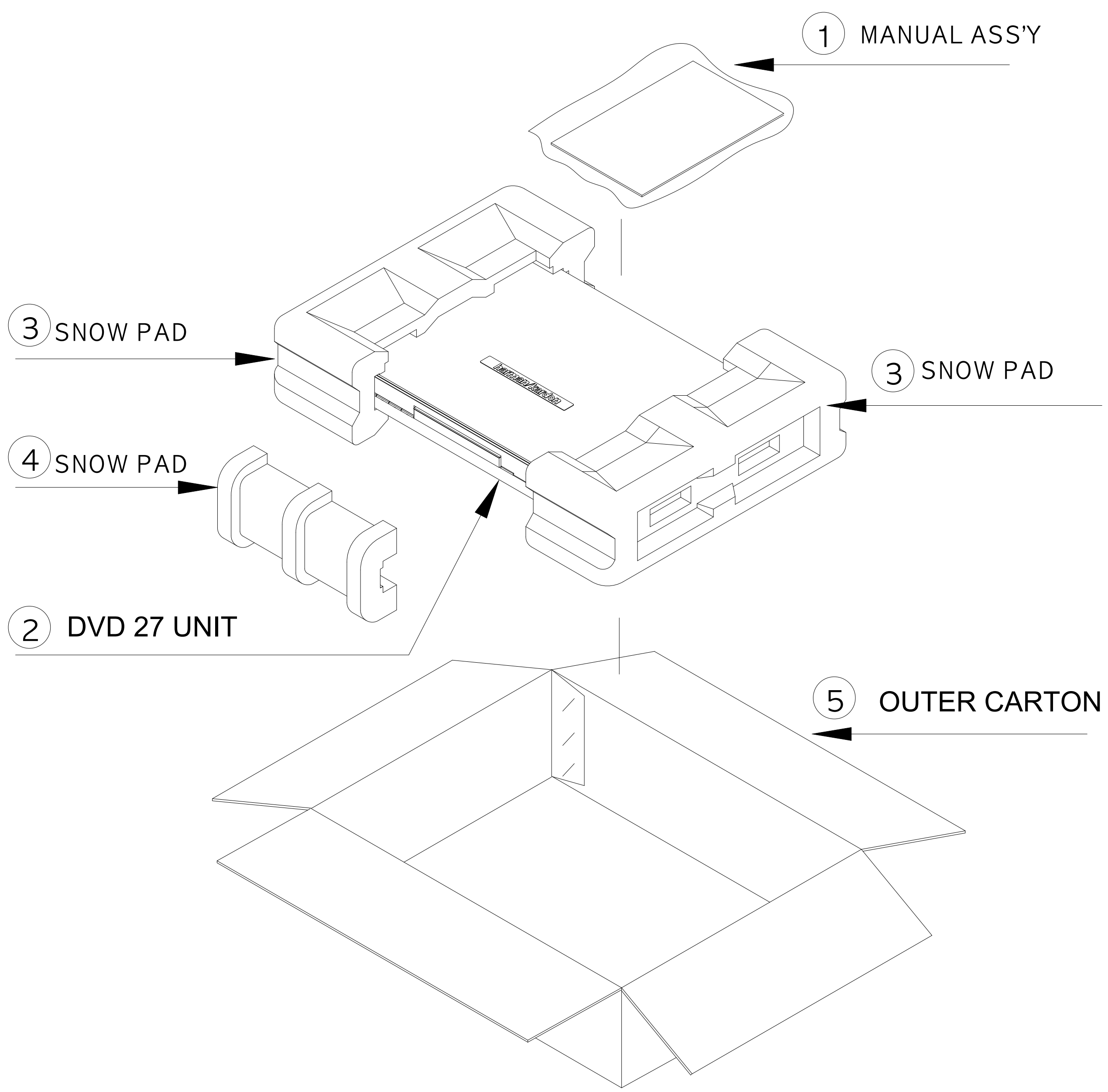
1. Instruction manual ass'y - Accessories





NO	DESCRIPTION	PARTS NO.	Q,ty
1	POLY BAG		1
2	CARD WARRANTY	CQE1A172X	1
3	HARMAN IMAGE BROCHURES	HQE1A273Z	1
4	INSTRUCTION MANUAL	CQX1A1048Z	1
5	BATTERY		2
6	REMOCON ASS'Y	CARTDVD27	1
7	CORD,PIN(3P,W/R/Y)	CJS4S004Z	1
8	CABLE,S-VHS(1.5M)	CJS0I006Z	1
9	CORD,JACK(MONO)1200MM	CJS9D002Z	1
10	STAPLE		3

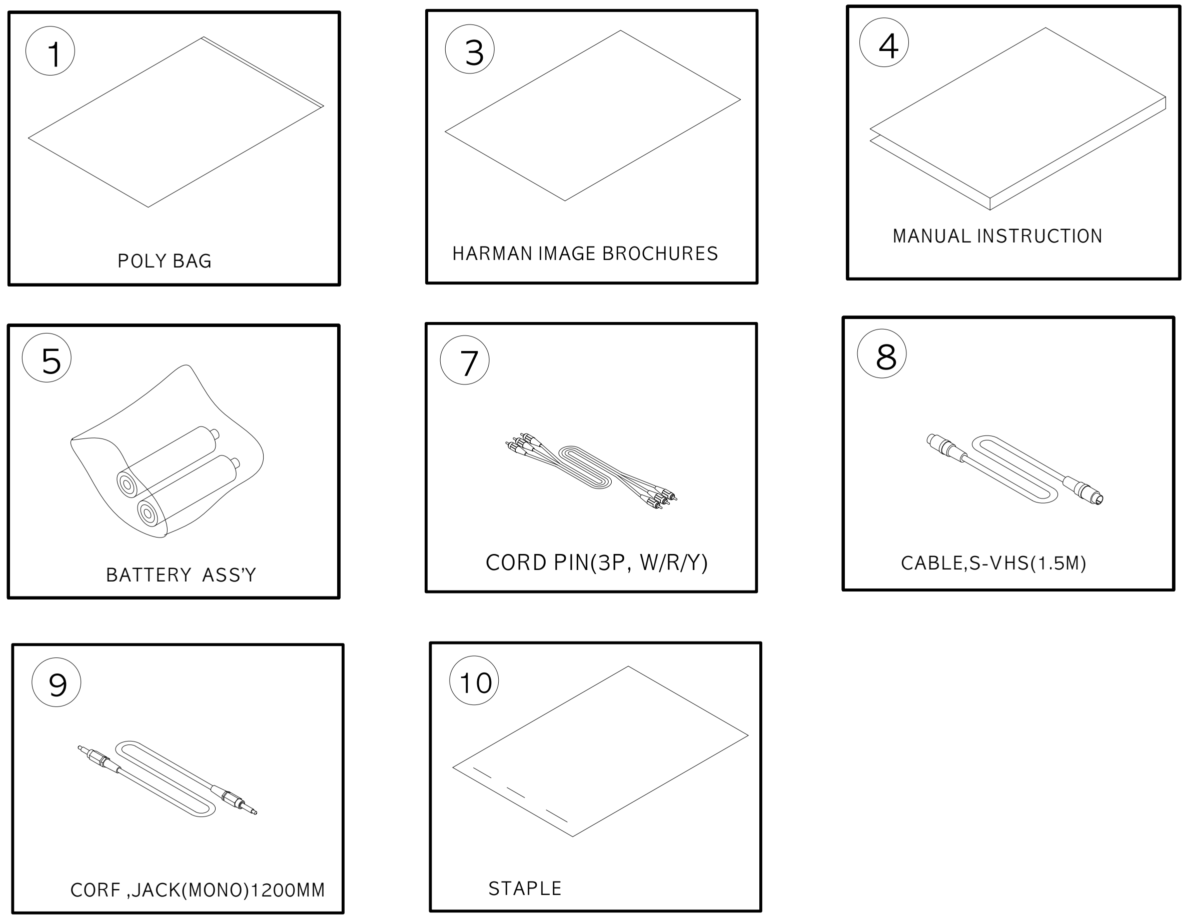
2. Package Drawing



NO	DESCRIPTION	PARTS NO.	Q,ty
1	MANUAL ASS'Y		1
2	DVD UNIT	DVD 27	1
3	SNOW,PAD	CPS1A714	2
4	SNOW,PAD	CPS1A715	1
5	OUTER CARTON	CPG1A798Z	1
6			
7			

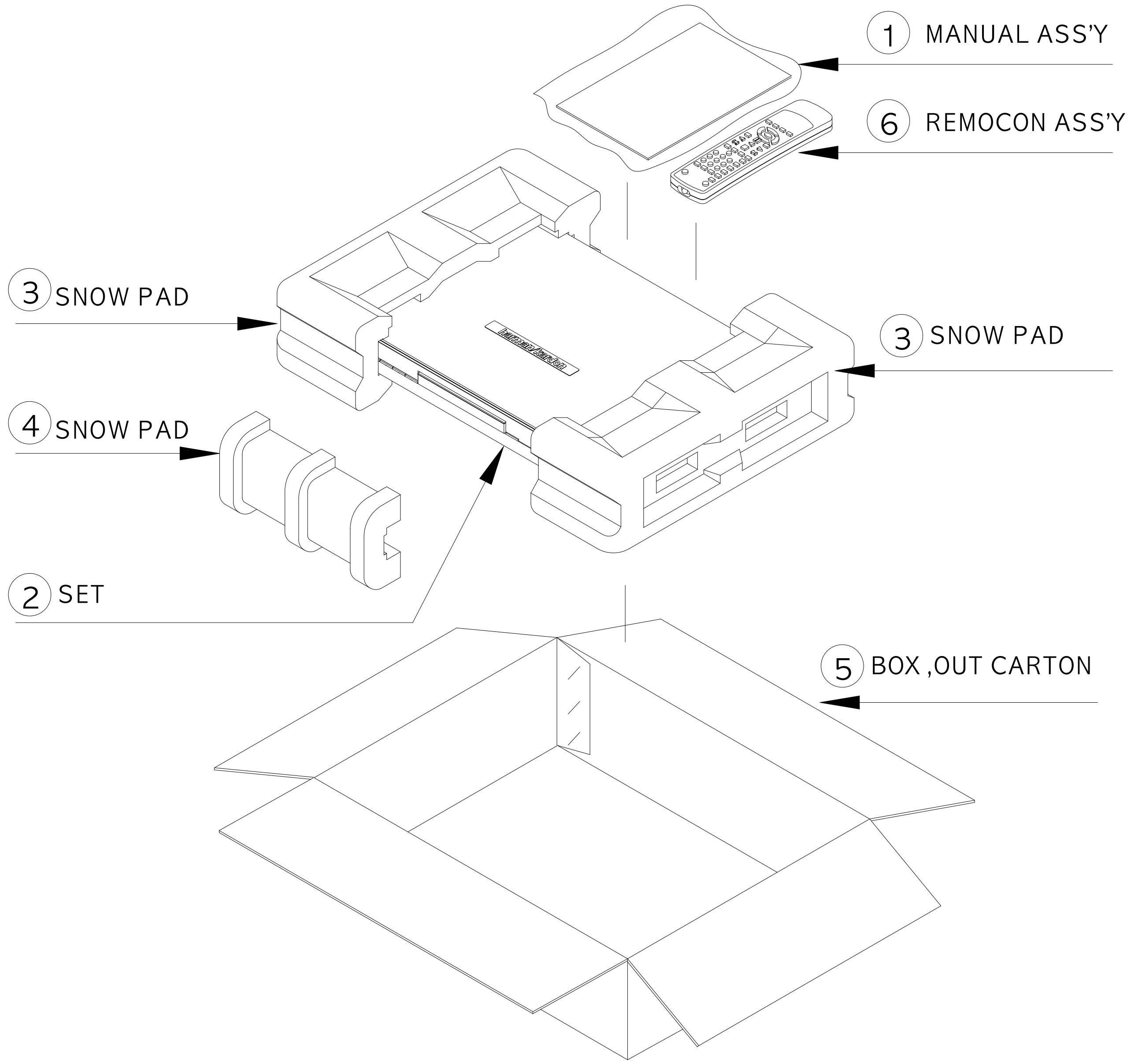
DVD27/230

1. Instruction manual ass'y - Accessories



NO	DESCRIPTION	PARTS NO.	Q,ty
1	POLY BAG		1
2			
3	HARMAN IMAGE BROCHURES	HQE1A273Z	1
4	INSTRUCTION MANUAL	CQX1A1051Z	1
5	BATTERY		2
6			
7	CORD,PIN(3P,W/R/Y)	CJS4S004Z	1
8	CABLE,S-VHS(1.5M)	CJS0I006Z	1
9	CORD,JACK(MONO)1200MM	CJS9D002Z	1
10	STAPLE		3

2. Package Drawing



NO	DESCRIPTION	PARTS NO.	Q,ty
1	MANUAL ASS'Y	CQXDVD27	1
2	SET	DVD27/230SET	1
3	SNOW,PAD	CPS1A714	2
4	SNOW,PAD	CPS1A715	1
5	BOX,OUT CARTON	CPG1A798W	1
6	REMOCON ASS'Y	CARTDVD27	1
7			

MODEL NAME : ☐ DVD27 ☐ DVD27/230 MP Release

Description : Characteristics Specification of Analog Audio L / R (2CH.)

Test Disc : TDV-540A (ABEX) , YEDS7 (Sony)

Test Conditions : 10kΩ Load Terminated , Must to be connect AP GND with set chassis.

AC Input : For USA (120V/60Hz) , For Europe (230V/50Hz)

Test Measuerment : CASCADE SYS-2522 (A.P)

1.ANALOG AUDIO OUTPUT Serial No. :

Measurement Item			Limit	Norminal	TEST DISC
Output Level [Vrms] 1KHz 0dB Playback		L		2.02	YEDS7 (SONY) TRACK 1
		R		2.02	
Level difference [Vrms]			< 0.2	0	
F/ response [dB] Reference 1KHz 0dB BW : 10Hz~500KHz Filter : None	2 0 Hz	L	0 ± 1.0	-0.01	YEDS7 (SONY) TRACK 2
		R		-0.01	
	100 Hz	L	0 ± 1.0	-0.01	YEDS7 (SONY) TRACK 4
		R		-0.01	
	10 KHz	L	0 ± 1.0	-0.03	YEDS7 (SONY) TRACK 10
		R		-0.03	
	2 0 KHz	L	0 ± 1.0	-0.14	YEDS7 (SONY) TRACK 13
		R		-0.14	
	4 4 KHz	L	0 ± 1.5	-1.05	TDV-540A (ABEX) T4,C16 AU3
		R		-1.05	
Emphasis Characteristic[dB] Ref.1kHz 0dB BW : 22Hz~22KHz	5 KHz	L	-4.53±1.0	-4.55	YEDS7 (SONY) TRACK 40
		R		-4.55	
	1 6 KHz	L	-9.04 ± 1.0	-9.03	YEDS7 (SONY) TRACK 41
		R		-9.03	
S/N [dB] 22~22KHz Aweighted		L	> 105	-120.8	YEDS7 (SONY) TRACK 23
		R		-120.8	
Channel Separation [dB] 1KHz 0dB Playback	1KHz Bandpass	L → R	> 95	-120.5	YEDS7 (SONY) TRACK 30 , 34
		R → L		-120.5	
Linearity [dB] -90dB playback	BW : 22Hz~22KHz	L	-89.5±3	-89.5	YEDS7 (SONY) TRACK 22
		R		-89.5	
T.H.D [%] 1KHz 0dB Playback	BW : 22Hz~22KHz	L	< 0.005	0.0015	YEDS7 (SONY) TRACK 1
		R		0.0015	
Dynamic Range [dB] CD-DA 1KHz -60dB	20KHz AES17	L	> 90	97.7	YEDS7 (SONY) TRACK 20
		R		97.7	
T.H.D [%] D V D 9 6 k	BW : 22Hz~22KHz	L	< 0.005	0.001	TDV-540A (ABEX) T3, C1
		R		0.001	
Dynamic Range [dB] D V D 9 6 k	BW : 20KHz AES17	L	> 90	104.3	TDV-540A (ABEX) T3, C2
		R		104.3	
T.H.D [%] D V D 48 k	BW : 22Hz~22KHz	L	< 0.005	0.001	TDV-540A (ABEX) T2, C1 , AU2
		R		0.001	
Dynamic Range [dB] D V D 48 k	20KHz AES17	L	> 90	105.3	TDV-540A (ABEX) T2, C2 , AU2
		R		105.3	

2. DIGITAL OUT

1) OPTICAL OUT (BW : 50Hz~100KHz) Peak to Peak

JITTER 44.1KHz (mUI)		< 50mUI	7.2	Normal 44.1KHz CD Playback
JITTER 96KHz (mUI)		< 50mUI	13.6	Normal 96KHz DVD Playback

2) COAXIAL OUT

Output Level [mV] Peak to Peak Level at 75ohm load terminated		500+50 (mV)	525	Normal CD or DVD Playback

Harman / Kardon

MODEL NAME : ☐ DVD27 ☐ DVD27/230 MP Release

Description : Characteristics Specification of Video
Test Disc : TDV-540A (ABEX) , MDVD-111 (TEAC) Serial NO.:
Test Conditions : 75Ω Load Terminated
AC Input : For USA (120V/60Hz) , For Europe (230V/50Hz)
Test Measuerment : VM-700T

1. Video Level Test (75Ω Terminated)

Measurement Item		Limit	Norminal	Test Disc
Video output [V]	Composite	1.0V ± 0.1V	1.02	MDVD-111 TITLE2,CHAPTER1 100% Color BAR
	S-Video Y	1.0V ± 0.1V	1.02	
	S-Video C	286mV ± 30mV	290	
	Component Y	1.0V ± 0.1V	1.03	
	Component Pb	700mV ± 70mV	680	
	Component Pr	700mV ± 70mV	680	
	Scart CVBS	1.0V ± 0.1V	1.02	
	Scart Red	700mV ± 70mV	720	
	Scart Green	700mV ± 70mV	720	
	Scart Blue	700mV ± 70mV	720	

** Pb/Pr & RGB Video Level check before please setting the Black Level off in the setup menu **

2. Video S/N Raito Test (75Ω Terminated)

Measurement Item		Limit	Norminal	Test Disc
Video SNR [dB] 100KHz~4.2MHz Use SC Trap	Composite	≥ 65.0 dB	-73.5	TDV-540A TITLE2,CHAPTER4 50% White Color
	S-Video Y	≥ 65.0 dB	-73.9	
	Component Y	≥ 65.0 dB	-73.1	
	Component Pb	≥ 65.0 dB	-73.7	
	Component Pr	≥ 65.0 dB	-73.7	

3. Chroma Signal AM.PM Test (75Ω Terminated)

Measurement Item		Limit	Norminal	Test Disc
Chroma AM [dB] 10KHz~500KHz	Composite Chroma	≥ 65.0 dB	-74.1	TDV-540A TITLE2,CHAPTER17 100% Magenta Color
	S-Video Chroma	≥ 65.0 dB	-74.1	
Chroma PM [dB] 10KHz~500KHz	Composite Chroma	≥ 60.0 dB	-65.3	
	S-Video Chroma	≥ 60.0 dB	-65.3	

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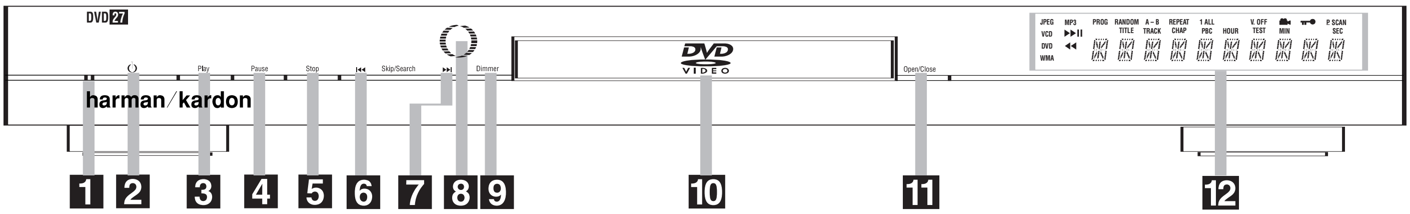
4. Video Frequency Respoens (75Ω Terminated)

Measurement Item		Limit	Norminal	Test Disc
Composite [dB]	0.5MHz 0dB Ref.	0		MDVD-111 TITLE2,CHAPTER8 100% Multi Brust
	1MHz	0dB ± 2dB	0.11	
	2MHz	0dB ± 2dB	0.11	
	3MHz	0dB ± 2dB	0.37	
	4MHz	0dB ± 2dB	0.66	
	5.8MHz	0dB ± 3dB	1.02	

Measurement Item		Limit	Norminal	Test Disc
S-Video Y [dB]	0.5MHz 0dB Ref.	0		MDVD-111 TITLE2,CHAPTER8 100% Multi Brust
	1MHz	0dB ± 2dB	0.03	
	2MHz	0dB ± 2dB	0.04	
	3MHz	0dB ± 2dB	0.27	
	4MHz	0dB ± 2dB	0.53	
	5.8MHz	0dB ± 3dB	0.83	

Measurement Item		Limit	Norminal	Test Disc
Component Y [dB] Interace Mode	0.5MHz 0dB Ref.	0		MDVD-111 TITLE2,CHAPTER8 100% Multi Brust
	1MHz	0dB ± 2dB	0.04	
	2MHz	0dB ± 2dB	0.08	
	3MHz	0dB ± 2dB	0.08	
	4MHz	0dB ± 2dB	0.17	
	5.8MHz	0dB ± 3dB	0.83	

FRONT-PANEL CONTROLS



NOTE: To make it easier to follow the instructions that refer to the controls and connectors in this illustration, a larger copy may be downloaded from the Product Support section for this product at www.harmankardon.com.

1 Power Indicator
2 Power On/Off (Standby)
3 Play
4 Pause
5 Stop
6 Skip/Search Reverse
7 Skip/Search Forward
8 Remote Sensor
9 Display Dimmer
10 Disc Drawer
11 Open/Close
12 Information Display

1 **Power Indicator:** This indicator lights amber when the unit is connected to an AC power source, but is not turned on. When the unit is on, the indicator lights blue.

2 **Power On/Off (Standby):** Press the button once to turn the DVD 27 on. Press it again to put the unit in the Standby mode.

3 **Play:** Press to initiate playback or to resume playback after the **Pause Button** 4 13 has been pressed.

4 **Pause:** Press this button to momentarily pause playback. To resume playback, press the button again. If a DVD is playing, action will freeze and a still picture will be displayed when the button is pressed.

5 **Stop:** Press this button once to place the disc in the Resume mode, which means that playback will stop, but as long as the tray is not opened or the disc changed, playback will continue from the same point on the disc when the **Play Button** 3 17 is pressed again. Resume will also work if the unit was turned off. Resume will not operate for WMA files or VCDs that do not have playback control. To stop a disc and have play start from the beginning, press the button twice.

6 **Skip/Search Reverse:** Press this button once to return to the start of the current chapter for a DVD or track for a CD. Subsequent individual presses will skip backwards through the available chapters or tracks. Press and hold the button to play the disc in the fast reverse mode at the speed indicated in the on-screen display and by the **Playback Mode Indicators** L.

7 **Skip/Search Forward:** Press this button once to move to the start of the next chapter for a DVD or track for a CD. Subsequent presses will skip forward through the available chapters or tracks. Press and hold the button to play the disc in the Fast Play mode at the speed indicated in the on-screen display and by the **Playback Mode Indicators** L.

8 **Remote Sensor:** The sensor that receives commands from the remote control is behind the front panel in this area. To ensure proper operation of the player with the remote, it is important that this area not be covered. In the event that the player is enclosed in a cabinet or if the remote sensor is covered, you may extend the remote sensor by connecting an optional, external remote sensor to the **Remote Control Input** ❷ on the rear panel (see page 12). When optional, external IR "blasters" are used for system control, they should be positioned so that they point at this area.

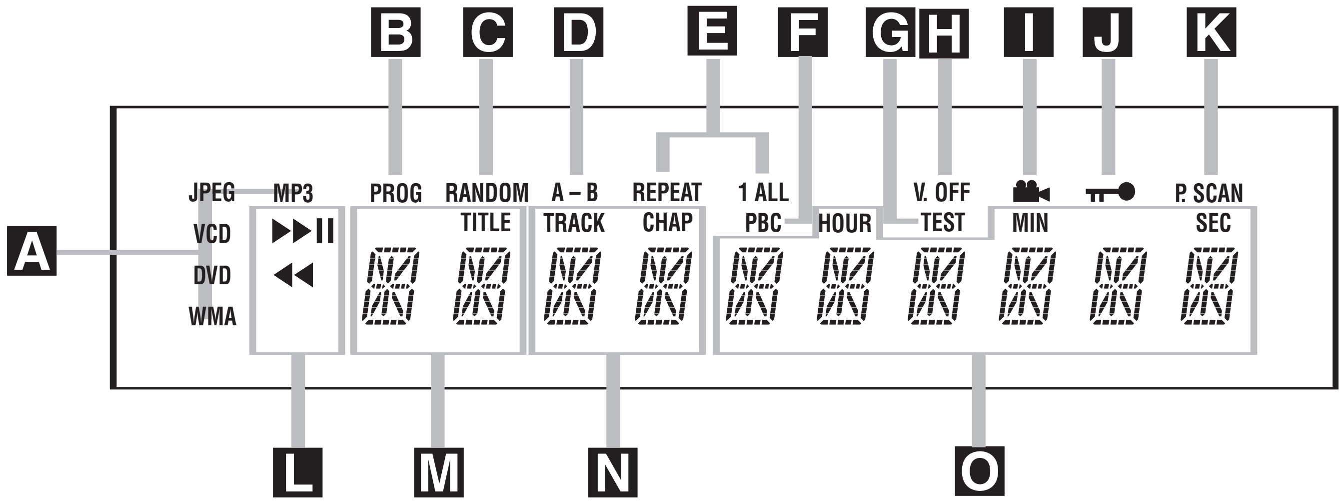
9 **Display Dimmer:** Press this button to reduce the brightness of the **Information Display** 12 by 50% or to turn the display off completely in the following order: FULL BRIGHTNESS ➔ HALF BRIGHTNESS ➔ OFF ➔ FULL BRIGHTNESS.

10 **Disc Drawer:** This drawer is used to hold the discs played in the unit. Be certain to seat all discs carefully within the recess in the drawer. Do not press down on the drawer when it is open, to avoid damage to the player. When the drawer is left open with no activity for 5 minutes, it will automatically close to prevent dust or dirt from entering the component, and to prevent accidental damage. If a disc is present, the DVD 27 will immediately begin playback.

11 **Open/Close:** Press this button to open or close the disc tray.

12 **Information Display:** The Information Display provides status information on the player and the disc being played through a series of specific indicators and messages that appear in the display. See page 8 for more information on the display.

FRONT-PANEL INFORMATION DISPLAY



NOTE: To make it easier to follow the instructions that refer to the controls and connectors in this illustration, a larger copy may be downloaded from the Product Support section for this product at www.harmankardon.com.

- **A** Disc-Type Indicators
- **B** Program Indicator
- **C** Random Indicator
- **D** A-B Repeat Indicator
- **E** Repeat Indicators
- **F** VCD Playback Control Indicator
- **G** Test Screen Indicator
- **H** V-OFF Indicator
- **I** Angle Indicator
- **J** Parental Lock Indicator
- **K** Progressive Scan Indicator
- **L** Playback-Mode Indicator
- **M** Title Indicators
- **N** Chapter/Track Number Indicators
- **O** Time Indicators

A Disc Type Indicators: The **DVD**, **CD**, **VCD**, **MP3**, **WMA** or **JPEG** indicator will light to show the type of disc currently being played.

B Program Indicator: This indicator lights when a playlist has been programmed using the menu system (available for CDs only). See page 33 for more information on programming playlists.

C Random Indicator: This indicator lights when the unit is in the Random Play mode.

D A-B Repeat Indicator: This indicator lights when a specific passage for repeat playback has been selected.

E Repeat Indicators: These indicators light when any of the Repeat functions are in use.

F VCD Playback Control Indicator: This indicator lights when the playback control function is turned on for VCDs.

G Test Screen Indicator: This indicator lights when the video test screen has been activated from within the Video submenu.

H V-OFF Indicator: This indicator lights in red when the unit's video output has been turned off by pressing the **V-OFF Button** ⑮ on the remote control.

I Angle Indicator: This indicator blinks when alternative viewing angles are available on the DVD currently playing.

J Parental Lock Indicator: This indicator lights in red when the parental-lock system is engaged in order to prevent anyone from changing the rating level without a code.

K Progressive Scan Indicator: This indicator lights when the unit sends out a progressive scan signal.

L Playback-Mode Indicators: These indicators light to show the current playback mode:

▶ Lights when a disc is playing in the normal mode. This indicator will flash when the disc is in Forward Slow Play mode. The on-screen banner display indicates the selected speed (1/2, 1/4, 1/8 or 1/16).

▶▶ When the DVD 27 is in the Fast Search play mode, two of these indicators will light to show that the unit is in a Fast Play mode. The on-screen banner display indicates the selected speed (x2, x4, x8, x20 or x100). Fast Play mode is not available for WMA files.

❙❙ Lights when the disc is paused.

◀◀ Lights when the disc is in the Fast Search Reverse mode. The on-screen banner display indicates the selected speed (x2, x4, x8, x20 or x100). Fast Search Reverse mode is not available for WMA files.

◀ Flashes when the disc is in Reverse Slow Play mode. The on-screen banner display indicates the selected speed (1/2 or 1/4).

M Title Indicators: These two positions in the display will show the current title number when a DVD disc is playing.

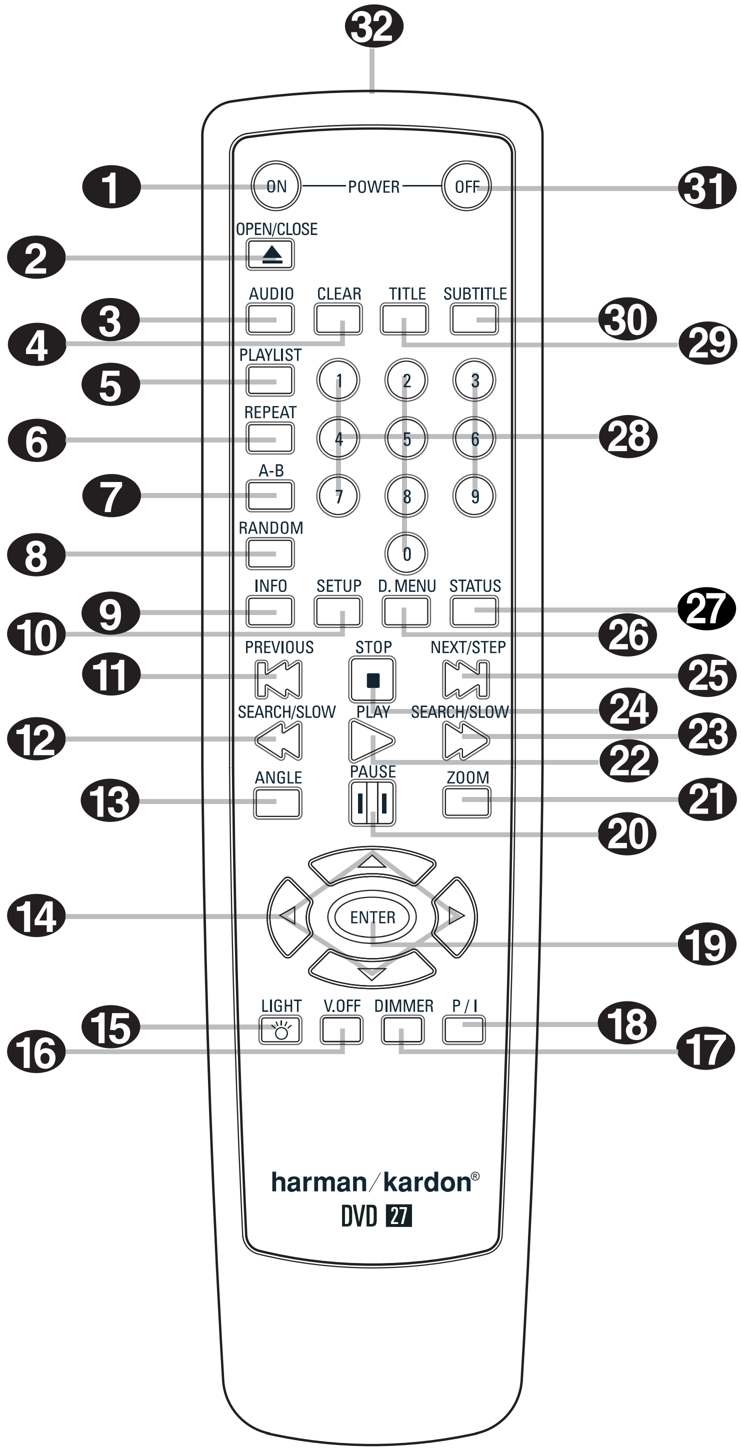
N Chapter/Track Number Indicators: When a DVD disc is playing, these two positions in the display will show the current chapter. When a CD disc is playing they will show the current track number.

O Time Indicators: These positions in the display will show the running time of a disc in play.

NOTE: The indicators **MNO** will also display text messages about the DVD's status, including `LOADING` when a disc is loading, `POWER OFF` when the unit is turned off, and `DISC ERROR` when a disc not compatible with the DVD is put into the play position.

REMOTE CONTROL FUNCTIONS

1 Power On
2 Open/Close
3 Audio Select
4 Clear
5 Playlist
6 Repeat
7 A-B Repeat
8 Random
9 Info
10 Setup
11 Previous Step/Skip
12 Search/Slow Reverse
13 Angle
14 ▲/▼/◀/▶ Navigation Buttons
15 Light
16 Video Off
17 Dimmer
18 Progressive Scan/Interlaced
19 Enter
20 Pause
21 Zoom
22 Play
23 Search/Slow Forward
24 Stop
25 Next Step/Skip
26 Disc Menu
27 Status
28 Numeric Keys
29 Title
30 Subtitle
31 Power Off
32 IR Emitter



NOTE: To make it easier to follow the instructions that refer to the controls and connectors in this illustration, a larger copy may be downloaded from the Product Support section for this product at www.harmankardon.com.

REMOTE CONTROL FUNCTIONS

❶ **Power On:** Turns on the player when it is in Standby mode (Harman Kardon logo appears on-screen).

❷ **Open/Close:** Press to open or close the disc tray.

❸ **Audio Select:** Press to access various audio languages on a DVD (if the DVD contains multiple audio streams). This button may also allow you to access other audio formats on DVD discs, such as linear PCM or Dolby Digital 5.1 tracks (or other formats), if they've been recorded on the disc.

❹ **Clear:** Press this button to remove on-screen menus or banners from the display screen. Press this button to clear the current play order displayed next to a track while programming a playlist. In Stop mode and with all menus and banners removed from the display, press and hold this button for five seconds to reset all settings to their factory defaults.

❺ **Playlist:** Press this button to access the Playlist on-screen menu, which enables you to change the order in which tracks are played on a CD. (See page 33 for more information on creating and playing playlists.)

❻ **Repeat:** Each press of this button changes the playback mode to repeat a chapter or track or the entire disc. A repeat icon will appear in the upper right corner of the screen indicating the current repeat mode. If the Player Information Screen is active, the changes will be displayed on screen.

❼ **A-B Repeat:** Press this button to enter the starting point of a section on a disc you wish to repeat. The second press enters the end of the selection to be repeated. Once the "A" (start) and "B" (end) points have been entered the player will repeat the selection until the **Play Button** ㉒ **3** is pressed or the disc is stopped. If the Player Information Screen is active, the changes will be displayed on screen.

❽ **Random:** Each press of this button starts or stops playback in random order. The Random function is only available when playing CDs, but not when a Playlist is active (the Player Information screen indicates Programmed Order on the Playlist line).

❾ **Info:** Press once to access the Player Information menu for information on the current disc and the playback mode settings. Press again to remove information from screen. See page 17 for more information on the Player Information menu.

❿ **Setup:** Press this button to use the DVD 27's on-screen menu system to adjust the player's configuration settings. Note that the **Info Button** ❾ must be pressed to access the DVD 27's Player Information menu to obtain detailed disc information, and to configure the playback mode of the disc.

⓫ **Previous Step/Skip:** Press this button once to skip back to the beginning of the current chapter on a DVD or track on a CD. Press it again to continue to skip back through the previous chapters or tracks. After first pressing the **Pause Button** ⑳, press this button to step backwards through a DVD or VCD as a series of still image frames.

⓬ **Search/Slow Reverse:** This button initiates fast or slow play in the reverse mode. For fast reverse play, each press of the button when playing DVD or VCD discs changes the speed as indicated by the number appearing in the upper right corner of the screen. For slow reverse play, first press the **Pause Button** ⑳ and each subsequent press of this button will change the slow play speed as indicated by the number appearing in the upper right corner of the screen.

⓭ **Angle:** Press this button to change the camera angle on discs programmed for multiple-angle views. When a JPEG is being displayed, pressing the **Angle Button** ⓭ repeatedly causes the on-screen image to rotate clockwise by 90 degrees each press. The current orientation in degrees will be displayed in the upper right corner of the screen.

⓮ ◀▶▲▼**Navigation Buttons:** Use to move the cursor in the on-screen menu system.

⓯ **Light:** Press to illuminate the buttons on the remote controller.

⓰ **Video Off:** Press this button to turn off the video output for improved audio performance when playing discs. Press it again to view the on-screen menus. It is highly recommended that you use this function to prevent "burn-in" of your plasma video display.

⓱ **Dimmer:** Press to change the brightness of the front panel display or to turn the display off completely in the following order: **FULL BRIGHTNESS ➔ HALF BRIGHTNESS ➔ OFF ➔ FULL BRIGHTNESS**

⓲ **Progressive Scan/Interlaced Button:** Each press of this button selects between the progressive scan and interlaced modes for the **Component Video Outputs** ❺.

⓳ **Enter:** Press this button to enter a setting in the DVD 27 menu system or to confirm a menu selection choice in a disc's on-screen menu.

⑳ **Pause:** Press this button to pause the disc and freeze the picture during DVD or VCD playback, or to pause the playback of a CD. To play a DVD or VCD in the slow, forward or reverse mode, first press this button and then press either the **Search/Slow Forward** ㉓ or **Reverse Button** ⓬.

㉑ **Zoom:** Press this button to zoom in on the image from a DVD, VCD or JPEG image. The image may be expanded by a factor of x2, x3, x4 or x5. Once the on-screen indication of the zoom ratio disappears from the screen you may use the **Navigation Buttons** ⓮ to explore the picture.

㉒ **Play:** Press this button to begin the playback of a disc, or to resume normal playback when a disc has been paused or scanned.

㉓ **Search/Slow Forward:** This button initiates fast or slow play in the forward mode. For fast forward play, each press of the button when playing DVD or VCD discs changes the speed as indicated by the number appearing in the upper right corner of the screen. For slow forward play, first press the **Pause Button** ⑳ and each subsequent press of this button will change the slow play speed as indicated by the number appearing in the upper right corner of the screen.

㉔ **Stop:** When a DVD is playing, press this button once to place the disc in the Resume mode, which means that playback will stop. However, as long as the disc drawer is not opened, playback will continue from the point where the disc was stopped when the **Play Button** ㉒ **3** is pressed again, as indicated by the LAST SCENE message (for DVDs) or the RESUME message (for CDs, MP3 files, JPEG files and VCDs with PBC) in the **Information Display** **12**. Resume will not operate for WMA files or VCDs that do not have playback control. Pressing the button twice will stop the disc and play will start from the beginning of the disc when the **Play Button** ㉒ **3** is pressed again.

㉕ **Next Step/Skip:** Press this button once to advance to the beginning of the next chapter on a DVD or track on a CD. Press it again to continue to advance through the remaining chapters or tracks. After first pressing the **Pause Button** ⑳, press this button to step through a DVD as a series of still-image frames.

㉖ **Disc Menu:** While a DVD is playing, press this button to view the disc's main menu.

㉗ **Status:** Press while a disc is playing to view the on-screen status banner display. The first press will display the current title and chapter, the play mode icon and the elapsed time, along with a "temperature bar" display of the time elapsed. You may use the ◀▶▲▼**Navigation Buttons** ⓮ and the **Enter Button** ⓳ to select and change the current title or chapter, or the time display. The Status Banner is only available for DVDs and VCDs when PBC is turned off. Press the button one more time to remove the status displays from the screen. More detailed information about the disc is available by pressing the **Info Button** ❾.

㉘ **Numeric Keys:** Press these buttons to enter a number.

REMOTE CONTROL FUNCTIONS

29 **Title:** When a DVD is playing, press this button to go back to the main title menu for the disc being played. If you are playing a DVD-Audio disc that contains other formats the DVD 27 is capable of playing, such as linear PCM or Dolby Digital 5.1, pressing this button may enable you to switch playback from one audio format to another.

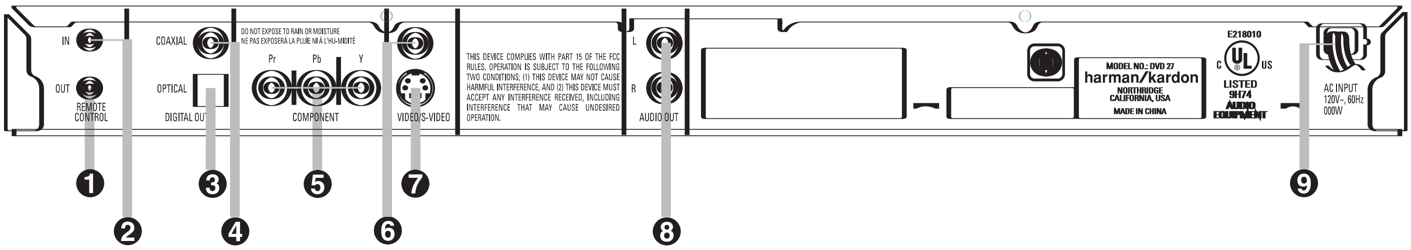
30 **Subtitle:** When a DVD is playing, press to select a subtitle language or to turn subtitles off.

NOTE: Due to the variations in how DVD discs are authored, the subtitle languages displayed by the DVD 27 may not accurately reflect the actual languages available on the disc. It is recommended that subtitles be selected using the disc's menu.

31 **Power Off:** Turns off the player to Standby mode.

32 **IR Emitter:** This small, clear button-like device sends the IR commands from the remote control to the DVD 27. To ensure proper performance of the remote control, be sure to point it toward the unit and do not cover it with your fingers when sending remote commands.

REAR-PANEL CONNECTIONS



NOTE: To make it easier to follow the instructions that refer to the controls and connectors in this illustration, a larger copy may be downloaded from the Product Support section for this product at www.harmankardon.com.

❶ Remote Control Output
❷ Remote Control Input
❸ Optical Digital Audio Output
❹ Coaxial Digital Audio Output
❺ Component Video Outputs
❻ Composite Video Output
❼ S-Video Output
❽ Analog Audio Outputs
❾ AC Power Cord

❶ **Remote Control Output:** Connect this jack to the infrared (IR) input jack of another compatible remote-controlled product to have the built-in Remote Sensor on the DVD 27 provide IR signals to other compatible products.

❷ **Remote Control Input:** Connect the output of a remote infrared sensor, or the remote control output of another compatible product, to this jack. This will enable the remote control to operate even when the front-panel Remote Sensor on the DVD 27 is blocked. This jack may also be used with compatible IR remote control-based automation systems.

❸ **Optical Digital Audio Output:** Connect this jack to the optical digital input of an A/V receiver or surround processor for Dolby Digital, DTS or PCM audio playback.

❹ **Coaxial Digital Audio Output:** Connect this jack to the coaxial digital input of an A/V receiver or surround processor for Dolby Digital, DTS or PCM audio playback.

NOTES:
- Connect either the **Optical Digital Audio Output** ❸ or the **Coaxial Digital Audio Output** ❹ to a corresponding digital audio input on your receiver or processor, but not both.
- The coaxial digital output should only be connected to a digital input. Even though it is the same RCA-type connector as standard analog audio connections, DO NOT connect it to a conventional analog input jack.

❺ **Component Video Outputs:** These outputs carry the component video signals for connection to display monitors with component video inputs. For standard analog TVs or projectors with inputs marked Y/Pr/Pb or Y/Cr/Cb, connect these outputs to the corresponding inputs. If you have a high-definition television or projector that is compatible with high-scan-rate progressive video (480p or better), connect these jacks to the HD component inputs. If you are using a progressive scan display device, PROGRESSIVE must be selected in the Video menu in order to take advantage of the progressive scan circuitry. See the "Scan Type" section on page 20 for more information on progressive scan video.

IMPORTANT: These jacks should NOT be connected to standard composite video inputs.

❻ **Composite Video Output:** Connect this jack to the video input on a television or video projector, or to a video input on an A/V receiver or processor if you are using that type of device for video input switching.

❼ **S-Video Output:** Connect this jack to the S-video input on a television or video projector, or to an S-video input on an A/V receiver or processor if you are using that type of device for S-video input switching.

❽ **Analog Audio Outputs:** Connect these jacks to an audio input on an A/V receiver, surround processor or your television for analog audio playback.

❾ **AC Power Cord:** Connect this plug to an AC outlet. If the outlet is controlled by a switch, make certain that it is in the ON position.

NOTE: You'll find more details about all audio/video connections under Setup and Connections on the following pages.

SETUP AND CONNECTIONS

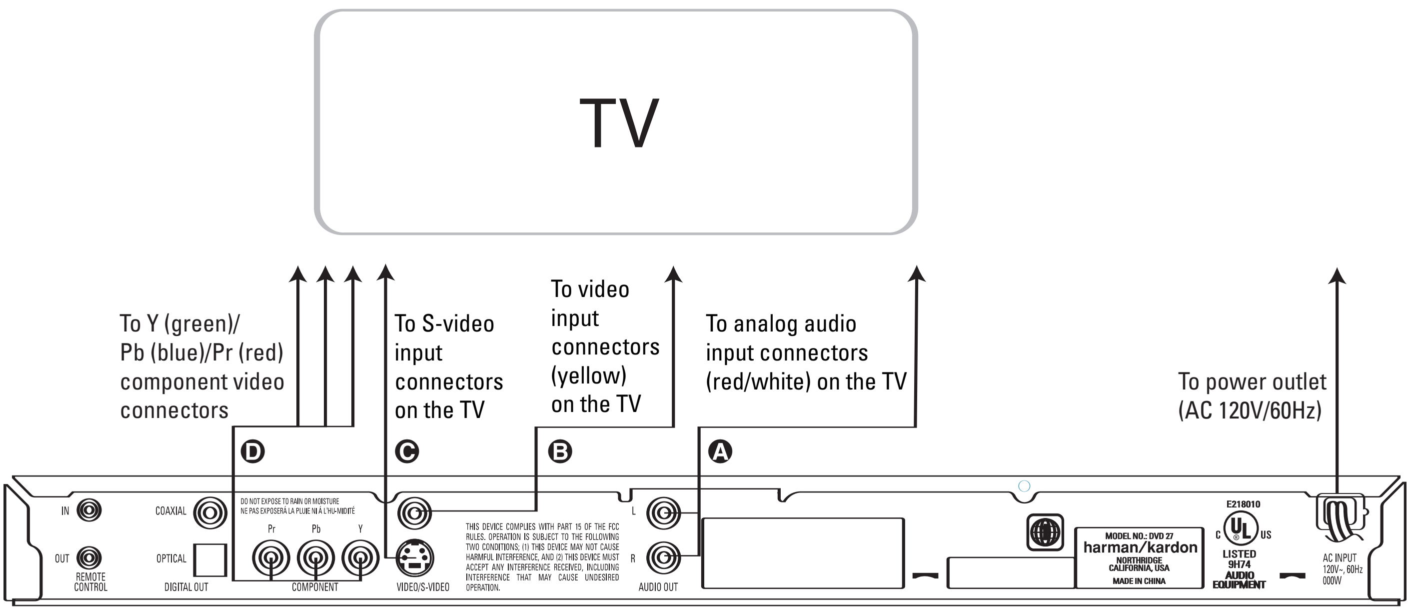
- Ensure that the power switch of this unit (and of other equipment to be connected) is set to "Off" before commencing connection. We also strongly recommend that you leave all system components unplugged from AC power until after you have completed the interconnections described in this section.
- Do not block the ventilation holes of any of the equipment and arrange them so that air can circulate freely.
- Read through the instructions before connecting other equipment.
- Ensure that you observe the color-coding when connecting audio and video cables.

VIDEO NOTES:

- While we suggest the use of component video for higher quality pictures, you may also use the standard S-video or composite video connection if your TV does not have component video inputs. The component and S-video outputs are not available simultaneously.
- The composite video output (yellow) combines the complete video signal (composite) and sends it to the TV (or to the A/V receiver) by one cable only. Use this video output when your TV set is equipped with a video input jack only.
- The S (separate) video output connector separates the color (C) and luminance (Y) signals before transmitting them to the TV set in order to achieve a sharper picture. Use the S-video cable when connecting the player to a TV equipped with an S-video input for improved picture clarity.
- The component video outputs further separate the color components of the video signal, optimizing the DVD 27's video performance. Component video connections are preferred, when available on your TV or receiver. If you are using a television or video display that is compatible with high-resolution 480P video signals, make sure to use the input jacks on the video display marked "HD Component," if available. Also, make sure to configure the display's input settings for use with "480P" video signals. You will also need to change the scan type in the DVD 27's Video Setup menu from "Interlaced" to "Progressive." See page 20.
- Modern audio/video receivers are capable of connection to several video source devices, such as the DVD 27 and a VCR, cable television set-top box, HDTV tuner or other device. The receiver is equipped with video monitor outputs for connection to your television, projector or plasma display. As you select any input source device, the receiver selects the correct video input and routes it to the correct video monitor output to your television. It is recommended that you connect one of the video outputs from the DVD 27 to the corresponding input on your receiver to simplify operation of your home entertainment system. Refer to the owner's guide for your receiver for more information.
- If your receiver is capable of multiroom operation, it is recommended that you connect both the component and composite video outputs of the DVD 27 to the receiver. This enables the highest-quality picture (component video) for viewing in the main listening room, while enabling the multiroom system, if it is video-capable, to distribute the composite video signal to the remote zone. Consult the owner's guide for your receiver to determine whether it has video multiroom capability.

Connecting to a TV Only

When using the DVD 27 with a television but no audio receiver or processor, connect it as follows. Make the **Analog Audio Connection A** and one of the **Video Connections** (**Composite Video B**, **S-Video C** or **Component Video D**). Remember to plug in the power cord.



SETUP AND CONNECTIONS

Connecting to a Receiver/Amplifier With a Dolby Digital or DTS Decoder

One of the major advantages of the DVD format is its ability to use a variety of digital audio formats for the ultimate in sonic performance. However, in order to enjoy the benefits of digital audio, you must use a receiver or processor that has digital audio decoding capabilities and make an optical or coaxial digital audio connection between the DVD 27 and your home theater system. This simple connection is made as shown below with an optional coax or optical cable. Only one of these connections is required, and both should not be made at the same time.

NOTES FOR ANALOG AUDIO:

- If you wish to use the DVD 27 as the input for a multiroom system, the **Analog Audio Outputs ❽** should be connected to the standard analog left/right DVD or CD inputs on your digital receiver or processor.
- The connection from the **Analog Audio Outputs ❽** to the TV is optional. If you plan on occasionally using your DVD 27 alone, without turning on your complete system, this connection must be made.
- When the audio signal is to be fed to an analog receiver rather than to the TV, connect the **Analog Audio Outputs ❽** to any analog audio inputs on your receiver or processor. The DVD 27 will “down-mix” Dolby Digital recordings to Dolby Pro Logic.
- The analog audio connection should also be made if you wish to play high-resolution 96kHz PCM audio discs where your receiver does not support 96kHz processing.

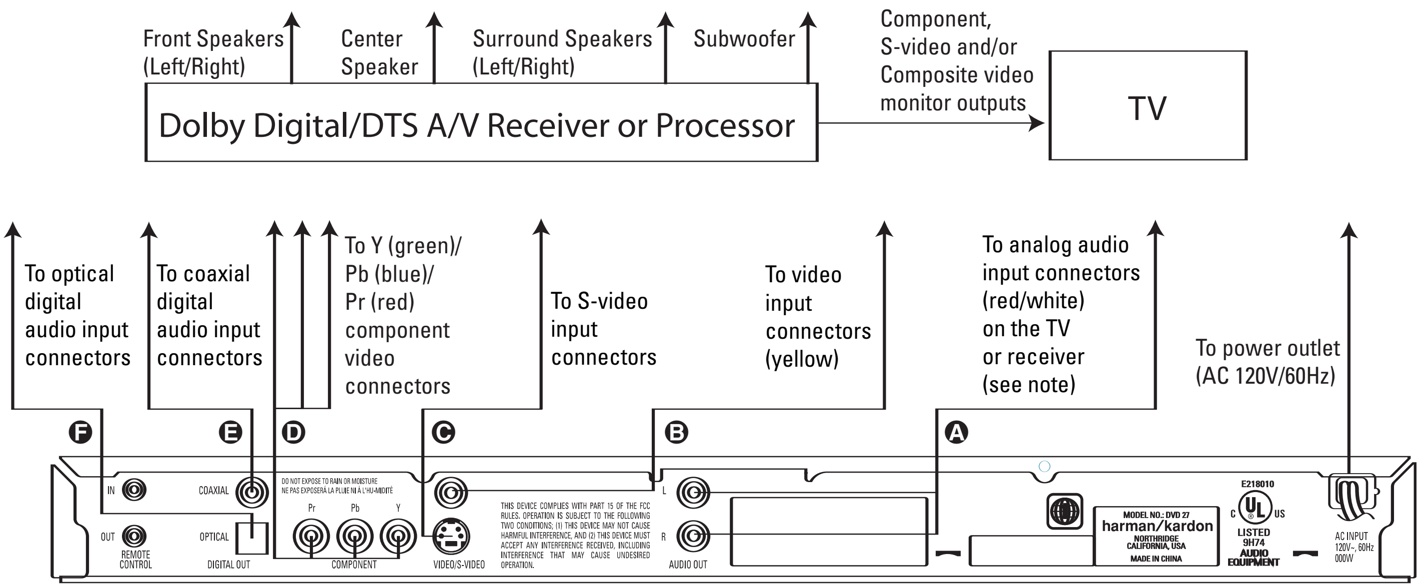
NOTE ON VIDEO: With multiple video sources, your audio/video receiver can be used for selecting the video signal and routing it to the TV. Connect the **Component ❺ Composite ❻** or **S-Video ❼** output of the DVD 27 to the correct video input on your receiver, and the video outputs of the receiver to your TV. For more details, see the manual for your audio/video receiver.

Connecting to a Receiver

When using the DVD 27 with an audio/video receiver or processor, connect it as follows. First, make one of the video connections (**S-video Ⓒ**, **Composite Video Ⓑ** or **Component Video Ⓓ**) to the video input jacks on the A/V receiver, and then connect the receiver’s video monitor output to the TV. If you will sometimes use the TV without the audio component, you may optionally make the **Analog Audio Connection Ⓐ** to the TV.

Second, make either the **Optical Digital Audio Connection Ⓕ** or the **Coaxial Digital Audio Connection Ⓔ**, to the receiver or processor. If your receiver/processor has multiroom capability, you may also connect the DVD 27’s analog audio outputs to the DVD analog audio inputs on the receiver.

IMPORTANT NOTE: Make certain that any device being connected, including the DVD 27, your receiver or processor and your TV or video display, is turned off whenever you make connections between products.



TEST SCREEN

DVD is one of the highest quality sources ever made available for in-home playback of prerecorded pictures and sound. In order to make certain that your home theater system is fully optimized to take advantage of DVD's superb picture quality, the DVD 27 offers a built-in video test signal that makes it easy to calibrate your TV or video display for proper playback.

Test Screen

With the test screen showing on your video display, the following adjustments may be made:

- The proper color intensity setting on your TV.
- Proper color adjustments using the color bars, which should be (left to right) black, white, yellow, cyan (turquoise), green, magenta, red, blue, black.
- The proper color transition, seen as sharp separation of the bars.
- The performance of the color circuits in your TV (with "Video" signals); bar edges should show no vertical crawling dots.

With the gray scale and the black/white fields below the color bars, the brightness and contrast of your screen can be adjusted.

NOTE: Most of the video adjustments using the DVD 27's test screen should be made using the controls on your video display, with the DVD 27's controls set at their factory default position in the center. If necessary, you may tweak the brightness and sharpness using the controls found in the DVD 27's video adjustments menu.

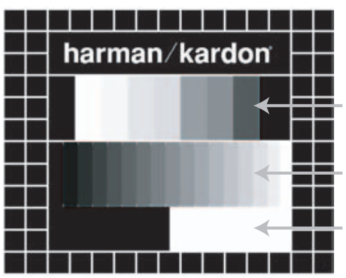


Figure 9

TV Picture Adjustment With Test Screen

Brightness Adjustment:

1. Turn down the color control on your TV until the color bars are visible in black and white.
2. Adjust the contrast on your TV to the lowest level where you still can see all bars within the gray scale in the test picture separately and clearly.
3. Adjust the brightness using the DVD 27 video adjustments control so that the bars in the gray scale are all visible. The bar furthest to the left has to be as black as possible rather than gray, but the next gradation must clearly be distinct from it. All the bars in the gray scale should be gradually and evenly changing from black to white, going from left to right.

Contrast Adjustment:

1. Adjust the contrast on your TV until you see a bright white bar in the lower right corner of the screen and a deep-dark-black bar to the left. The optimal contrast setting will depend on your preference and the surrounding light in the TV room.
2. If the brightness of the white bar no longer increases when the contrast is turned up or the borders of the white "harman/kardon" letters on top bloom (overlight) into the black areas (drastically decreasing the sharpness of the type), the contrast has been turned up too much. Reduce the contrast until these effects disappear and the video still looks realistic.
3. If you are watching TV with customary surrounding daylight, adjust the contrast so that a normal video picture has about the same look as the surroundings in your room. That way the eye is relaxed when watching the TV picture. This contrast setting may be reduced when the surrounding light is dimmed, thereby usually improving the sharpness of a video significantly.
4. The gray scale in the middle line needs to have the same clear difference between each bar as before the contrast adjustment. If not, go back to "Brightness Adjustment" and repeat Step 3 and then "Contrast Adjustment," making only minor adjustments each time for optimization.

Color Adjustment

1. When the brightness and contrast are set optimally, turn up the color control to the level of your preference. Adjust to the level where the colors look strong but still natural, not overdone. If the color level is too high, depending on the TV, some of the bars will seem wider or the color intensity will not increase while the control is turned up. Then the color control must be reduced again. Ultimately, you also should test the color intensity with a video – e.g., pictures of natural faces, flowers, fruit and vegetables, and other common natural articles for an optimal setting of the color intensity.
2. Use the large white bar below the gray scale to tweak the warmth of the picture. Every viewer has a preference as to how the glow of the picture should be. Some prefer a little colder picture, some a warmer glow. The Tint function on your TV and the white bar can be used to control this. Adjust the Tint to the level where you feel the white color has the tone you prefer.

Sharpness Adjustment

Contrary to intuition, the picture will appear sharper and clearer with the sharpness, or Edges, setting backed off from the maximum setting. Reduce the sharpness setting on your television, and the Edges setting on the DVD 27 video adjustments menu if necessary, to minimize the appearance of any white lines between the bars in the gray scale portion of the test screen.

Convergence and Edge Focus

The crosshatch pattern that surrounds the test screen may be used to evaluate edge focus and convergence in front- or rear-projection video displays. However, the controls used to adjust these parameters are often not user-accessible. In any event, these adjustments are extremely complex, and require proper training and experience to avoid worsening the situation. Therefore, it is recommended that if you are unable to improve the picture using the available controls, contact the video display manufacturer's authorized service representative for assistance.

When all desired setup and configuration entries have been made, use the ▲▼ **Navigation Buttons** ⓮ until "Done" is highlighted at the bottom of the Video Adjustments submenu. Press the **Enter Button** ⓳ to select it to return to the on-screen menu system. Then, press the **Setup Button** ⓾ to remove the menu displays from the screen. The unit will return to normal operation and you are ready to enjoy the finest in DVD or CD playback!

PLAYBACK BASICS

Loading Discs

To load discs in the DVD 27, first turn the DVD 27 on by pressing in the **Power On/Off Switch** 2 or **Power On Button** 1. Note that the **Power Indicator** 1 will turn amber when the unit is connected to an AC power source. It will turn blue when the **Power On Button** 2 1 is pressed.

Next, press the **Open/Close Button** 2 11 until the disc tray opens.

Hold the disc by the edge, and gently place it into the disc drawer, making certain that the disc is properly seated in the tray's insert. If the disc is not correctly centered, you may damage both the disc and the player when the drawer closes. When loading discs, please note the following:

- The DVD 27 will play discs with the following logos as well as most DVD-RW or DVD+RW discs and most WMA and JPEG discs, including Kodak Picture CDs, but not Kodak Photo CDs. DO NOT attempt to play another type of disc.

- The DVD 27 will only display video in the NTSC format. Although the PAL format is generally used in Europe and other regions of the world outside North America, some music or other DVDs are available in PAL format with a Region Code of "0," which means they may be played on any DVD player around the world. The DVD 27 will automatically detect if such a disc is in the PAL format, and make the necessary conversions so that the video may be displayed on an NTSC television. Note that PAL discs bearing a Region Code other than "0" or "1" may not be played on the DVD 27.
- Playback capability for CD-RW, DVD-RW, DVD-R, DVD+RW or DVD+R discs will vary according to the quality of the disc. On some occasions it is possible that these discs may not play on the DVD 27. This does not indicate any problem with the DVD 27.
- The DVD 27 will only play discs that are coded for Region 1 or discs that are open to being played in all regions (Region Code "0"). Discs that contain a Region Code of 2, 3, 4, 5 or 6 (as noted by a number inside a world map logo on the disc's cover jacket or case) will not play.
- Both 5-inch (12cm) and 3-inch (8cm) discs may be used.
- When loading CD audio discs, load the discs with the label side up.
- When loading DVD discs with printed labels, load them label side up.
- Some DVD discs are double-sided. The title information for these will be printed on the inner ring of the disc, very close to the center hole. The title for the side you wish to play should be facing up.

After a disc is properly loaded, press the **Open/Close Button** 2 11 to close the disc drawer. After the drawer closes, you will see a brief indication of LOADING in both the **Main Information Display** 12 and in the on-screen display to alert you to the fact that the unit is determining the type of disc (DVD, CD, VCD, JPEG, WMA or MP3) and is reading the data for track, chapter, title and other information about the disc.

Once the disc's data has been read, the type of disc will be displayed by the **Disc-Type Indicator** A and its type will be identified in the upper right corner of the screen. If the disc is a DVD, CD or VCD2.0 disc, it will automatically begin playing. The disc's track timing information and other relevant data will appear in the **Main Information Display** 12.

Any time a control button is pressed, an icon will appear in the upper right corner of the screen to indicate the player's action. These icons include the standard transport modes (play, stop, pause, forward and reverse fast and slow search, track skip), the open/close disc drawer symbol, the repeat and random modes, and the prohibit icon (Ø) if the command action is not available at that time or for that disc. As explained in more detail in other sections of this manual, pressing the **Status Button** 27 displays the Status Banner for DVDs, and pressing the **Info Button** 9 displays the Player Information menu.

- When a DVD is detected, playback will automatically begin and the screen will show the program or the disc's menu, depending on how the disc has been created.
- If a CD is detected, playback will begin automatically.
- If the disc contains MP3, WMA or JPEG files, or if it is a VCD without playback control, the Player Information display will appear (see Figure 10). To play one of these files, you may need to use the ▲▼◀▶ **Navigation Buttons** 14 to select a folder and press the **Enter Button** 19 to open it. Use the ▲▼ **Navigation Buttons** 14 to select a file for playback, and press the **Enter Button** 19 to begin play.
- VCD2.0 discs will begin play automatically, similar to a conventional audio CD.



Figure 10

If a disc is already in the drawer when the unit is turned on, it will begin playing. If the disc was stopped using the Resume function, playback will begin from the point where it was stopped. If the disc was stopped by pressing the **Stop Button** 5 24 twice, the disc will begin playing from its beginning.

Playback Features for DVD and CD Discs:

- To momentarily pause playback and freeze the current picture frame on a DVD, press the **Pause Button** 4 20. To resume playback after pressing the Pause button, press the **Play Button** 3 22.
- To move forward or backward through the tracks on a CD or the chapters on a DVD, press the **Skip Forward/Reverse Buttons** 6 7 on the front panel or the **Previous/Next Buttons** 11 25 on the remote.
- To move forward or backward through the DVD or CD disc being played at fast speed, press the **Search Forward/Reverse Buttons** 12 23, or press and hold the front-panel **Skip/Search Buttons** 6 7 briefly until fast play begins, and then release them. Once one of these buttons is pressed, the fast search will continue until the **Play Button** 3 22 is pressed. Each press of the **Search Forward/Reverse Buttons** 6 7 12 23 will cycle to the next speed in the following order: 2x, 4x, 8x, 20x, 100x.

NOTE: Fast search is available when MP3 discs are playing, but not for WMA files.

- When a DVD is playing, you may move forward or backward through the disc in slow motion by first pressing the **Pause Button** 4 20 and then pressing the **Search/Slow Forward** or **Search/Slow Reverse Buttons** 6 7 12 23. Each press of the buttons will cycle the player through one of the four forward slow-play speeds: 1/2x, 1/4x, 1/8x or 1/16x or one of the two reverse slow-play speeds: 1/2x or 1/4x. Press the **Play Button** 3 22 to resume normal playback.

Note that there is no audio playback during fast or slow-forward or -reverse play of DVD discs. This is normal for DVD, as A/V receivers and surround processors cannot process the digital audio streams

PLAYBACK BASICS

during slow modes. Slow-play is not available for CD discs.

- To advance frame by frame while a DVD is playing, first press the **Pause Button** **4** **20**, then press the **Skip/Step (Previous)** **6** **11** or **Skip/Step (Next)** **7** **25** buttons repeatedly. Press the **Pause** **4** **20** or **Play Button** **3** **22** to resume normal play. Frame-by-frame movement in reverse is not available.
- When a camera icon shows on the screen, or the **Angle Indicator** **I** appears, this is your indication that there is multiple-angle information on the disc being played. To change the angle, press the **Angle Button** **13** repeatedly until the desired angle view appears. An on-screen banner message will appear to indicate the angle view in use.

To illuminate the buttons on the remote control so that they may be seen in low-light conditions, press the **Light Button** **15**.

TROUBLESHOOTING GUIDE

TROUBLESHOOTING GUIDE

SYMPTOM	POSSIBLE CAUSE	SOLUTION
Unit does not turn on	• No AC power	• Check AC power plug and make certain any switched outlet is turned on.
Disc does not play	• Disc loaded improperly • Incorrect disc type • Invalid Region Code • Rating is above parental preset	• Load disc label-side up; align the disc with the guides and place it in its proper position. • Check to see that disc is CD, CD-R, CD-RW, VCD, MP3, WMA, JPEG, DVD-R, DVD-RW, DVD+R, DVD+RW (standard conforming) or DVD-Video; other types will not play. • Use Region 1 or Open Region (0) disc only. • Enter password to override or change rating settings (see page 18).
No picture	• Intermittent connections • Wrong input • Progressive Scan output selected • Video Off feature active	• Check all video connections. • Check input selection of TV or receiver. • Use Progressive Scan mode only with compatible TV. If needed, press the **Progressive Scan/Interlaced Button** ⓲ to toggle to the correct mode. • Press **Video Off Button** ⓰ to reactivate video circuitry (see page 27).
No sound	• Intermittent connections • Incorrect digital audio selection • DVD disc is in fast or slow mode • Surround receiver not compatible with 96kHz PCM audio	• Check all audio connections. • Check digital audio settings. • There is no audio playback on DVD discs during fast or slow modes. • Use analog audio outputs.
Picture is distorted or jumps during fast forward or reverse play	• MPEG-2 decoding	• It is a normal artifact of DVD playback for pictures to jump or show some distortion during rapid play.
Some remote buttons do not operate during DVD play; prohibited symbol ⃠ appears (see below)	• Function not permitted at this time	• With most discs, some functions are not permitted at certain times (e.g., Track Skip) or at all (e.g., direct audio track selection).
The OSD menu is in a foreign language	• Incorrect OSD language	• Change the display language selection (see page 20).
The ⃠ symbol appears	• Requested function not available at this time	• Certain functions may be disabled by the DVD itself during passages of a disc.
Picture is displayed in the wrong aspect ratio	• Incorrect match of aspect ratio settings to disc	• Change aspect ratio settings (see page 20).
Remote control inoperative	• Weak batteries • Sensor is blocked	• Change both batteries. • Clear path to sensor or use optional outboard remote sensor.
Disc will not copy to VCR	• Copy protection	• Many DVDs are encoded with copy protection to prevent copying to VCR.
Password not accepted.	• Incorrect password being used or password has been forgotten.	• Stop play of disc. Press and hold the **Clear Button** ❹ until the display blinks. This resets the password and all settings to their defaults.

DISASSEMBLY PROCEDURES (DVD 27 & DVD 27/230)

I TOP COVER (12) REMOVAL

1. Remove the 4 screws (S6) at rear and then remove the Top Cover.

II MECHANISM ASS'Y (10) REMOVAL

1. Short the LD Protect on the Mechanism out by using solder.
2. Disconnect the Card Cable (24P) on the Mechanism Ass'y (10) from connector (CN11) on the Main PCB Ass'y (18).
3. Disconnect the Lead Wire (6P) on the Mechanism Ass'y (10) from connector (CN13) on the Main PCB Ass'y (18).
4. Disconnect the Lead Wire (5P) on the Mechanism Ass'y (10) from connector (CN12) on the Main PCB Ass'y (18).
5. After open Tray by using Mechanism Tray Gear in the bottom side, remove the Tray Door (2).
6. Remove 2 screws (S1) of bottom side and then remove Mechanism Ass'y (10) from the Bottom Chassis (7).

III FRONT PANEL ASS'Y (5) REMOVAL

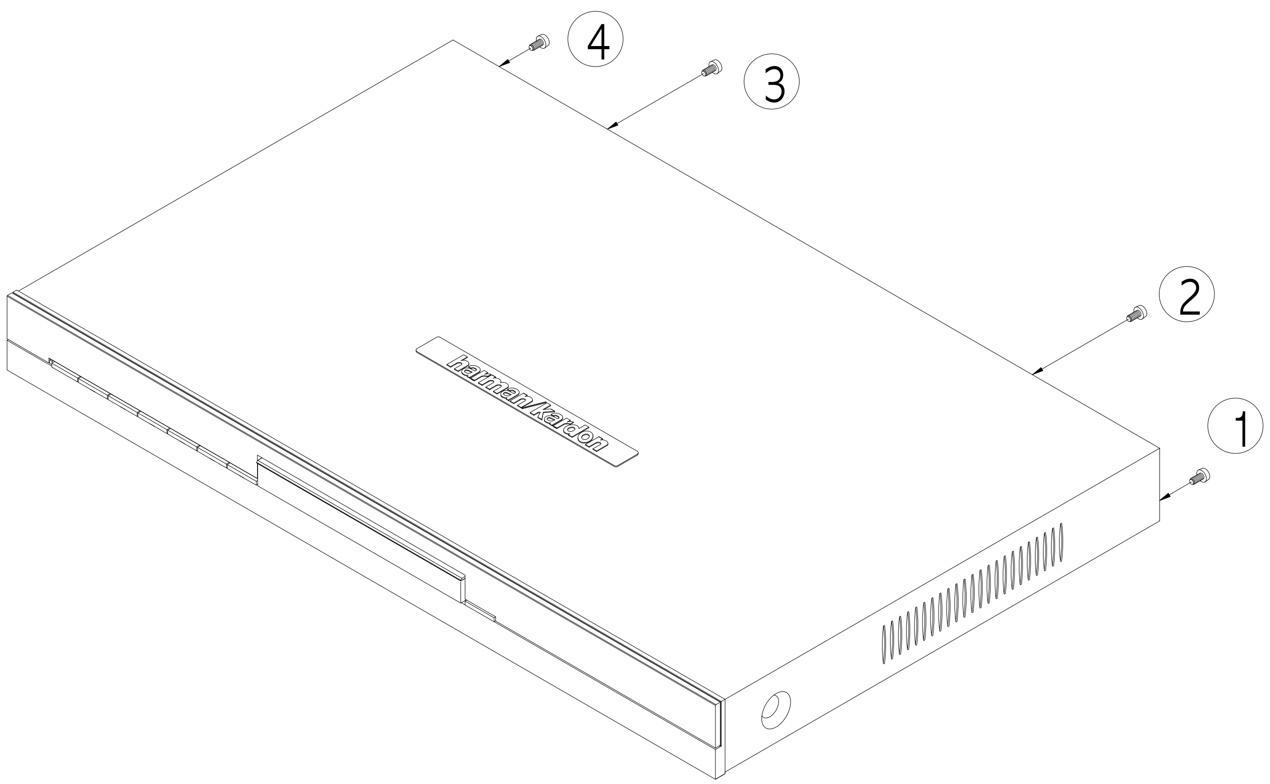
1. Disconnect the Card Cable (15P) on the Front PCB (17) from connector (CN04) on the Main PCB Ass'y (18).
2. Remove 2 screws (S5) of left & right outside.
3. Remove the Front Panel Ass'y (5) from the Bottom Chassis (7).
4. Remove 5 screws (S1) and then remove the Front PCB (17) from the Front Panel Ass'y (5).

IV MAIN PCB (18), SMPS PCB (19) & REAR PANEL (8) REMOVAL

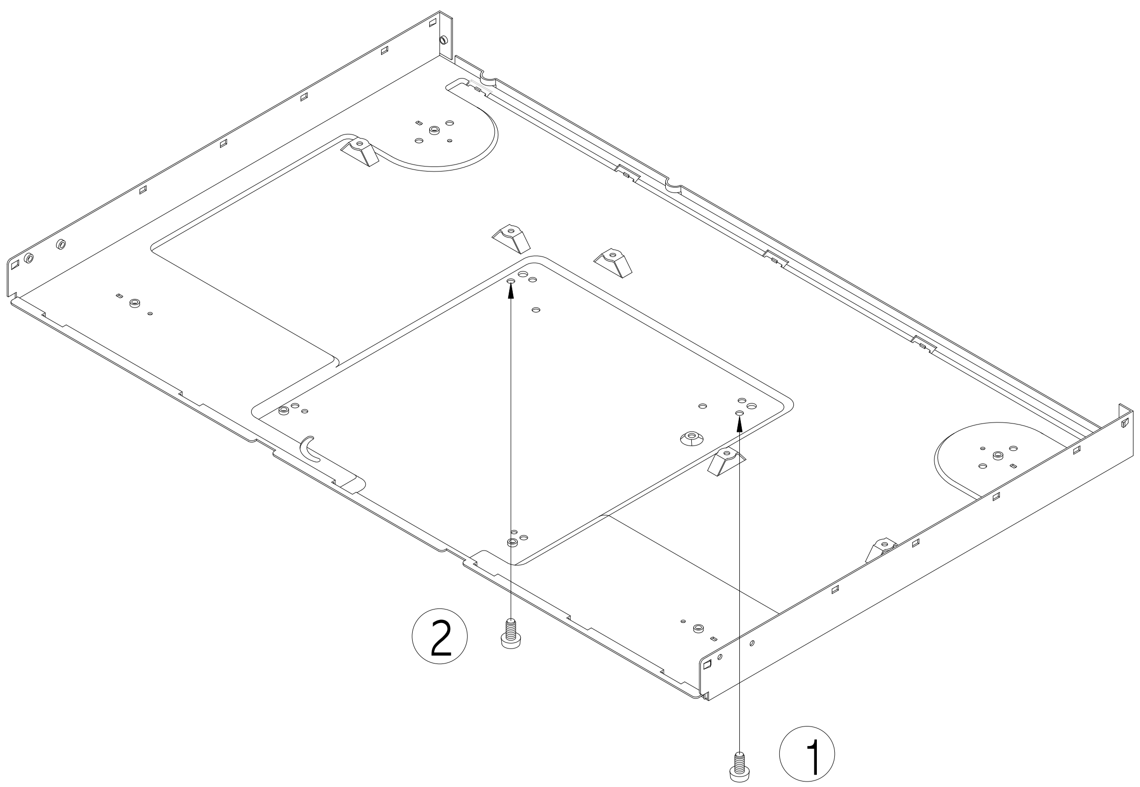
1. Remove the AC Power Cord (16).
2. Disconnect the lead wire (BN02-12P) on the SMPS PCB (19) from connector (CN02) on the Main PCB Ass'y (18).
3. Remove 5 screws (S4), 1 screw (S7)* & 5 screws (S2) and then remove the Main PCB (18) & the SMPS PCB (19).
4. Remove the Rear Panel (8) from the Bottom Chassis (7).

* "1 screw(S7) " is only applicable for the DVD 27/230.

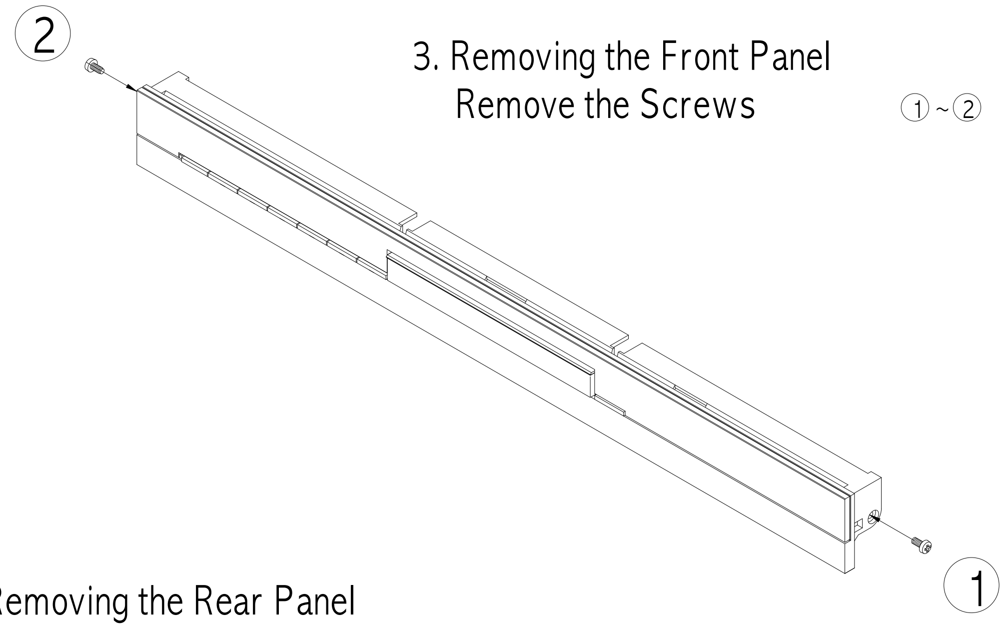
1. Removing the Top Cabinet
Remove the Screws ① ~ ④



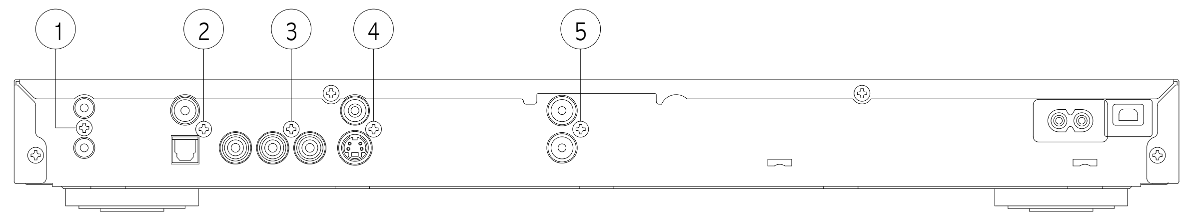
2. Removing the Bottom Chassis
Remove the Screws ① ~ ②



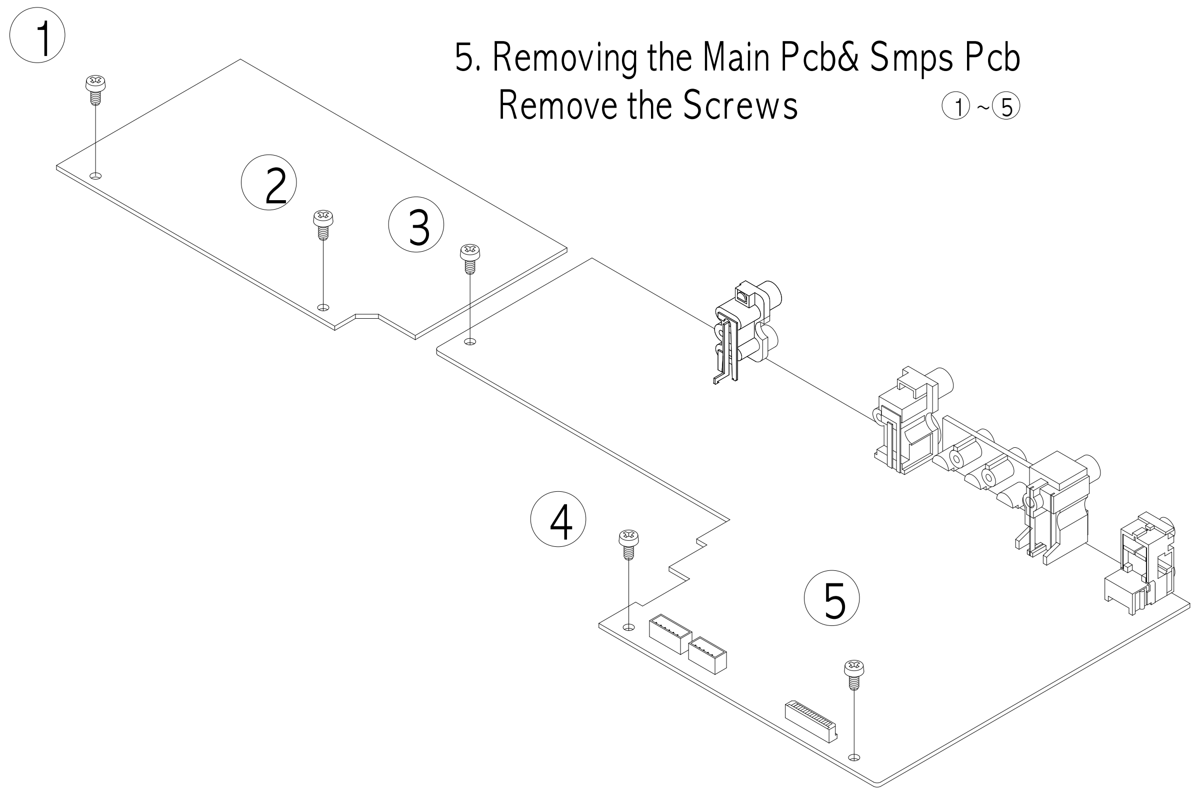
3. Removing the Front Panel
Remove the Screws ① ~ ②



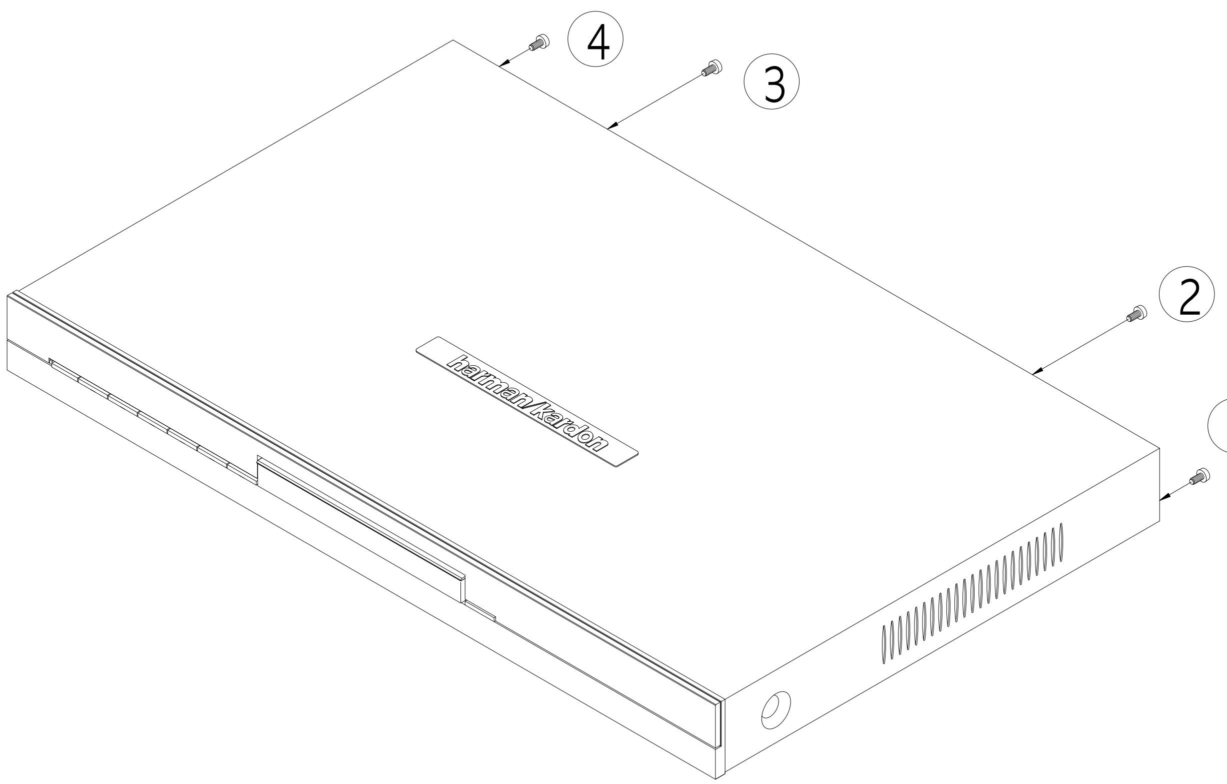
4. Removing the Rear Panel
Remove the Screws ① ~ ⑤



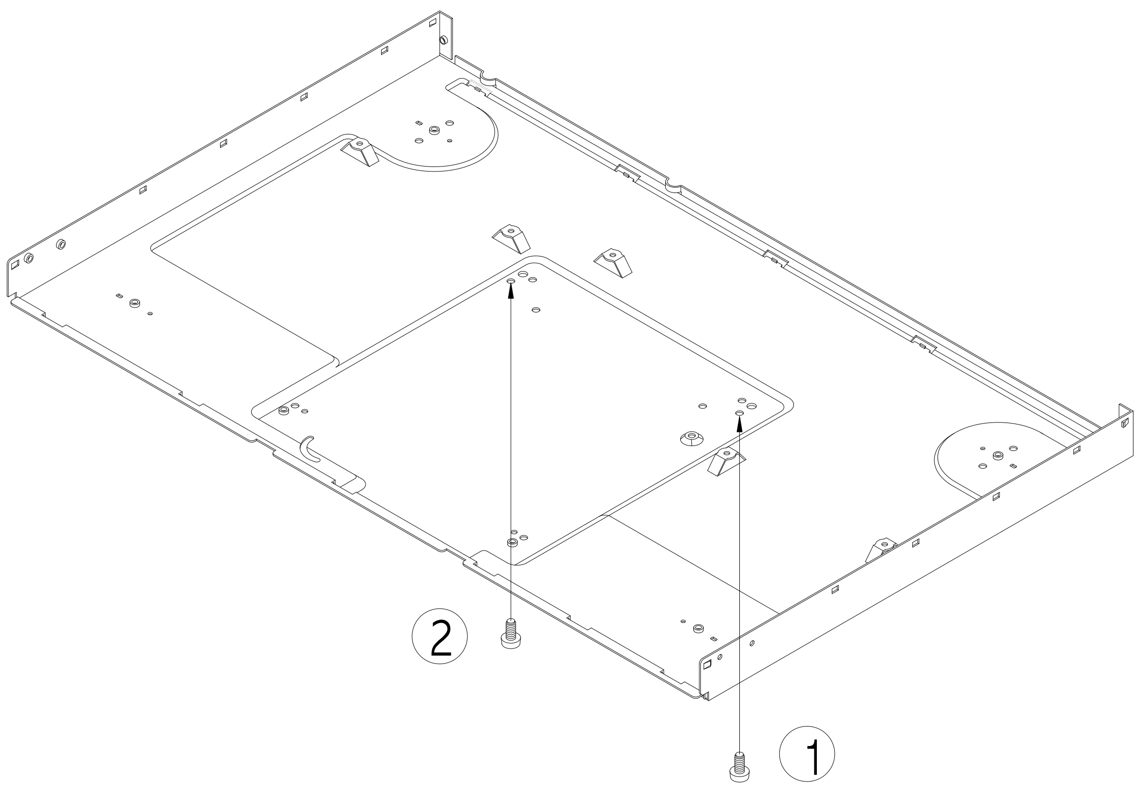
5. Removing the Main Pcb& Smps Pcb
Remove the Screws ① ~ ⑤



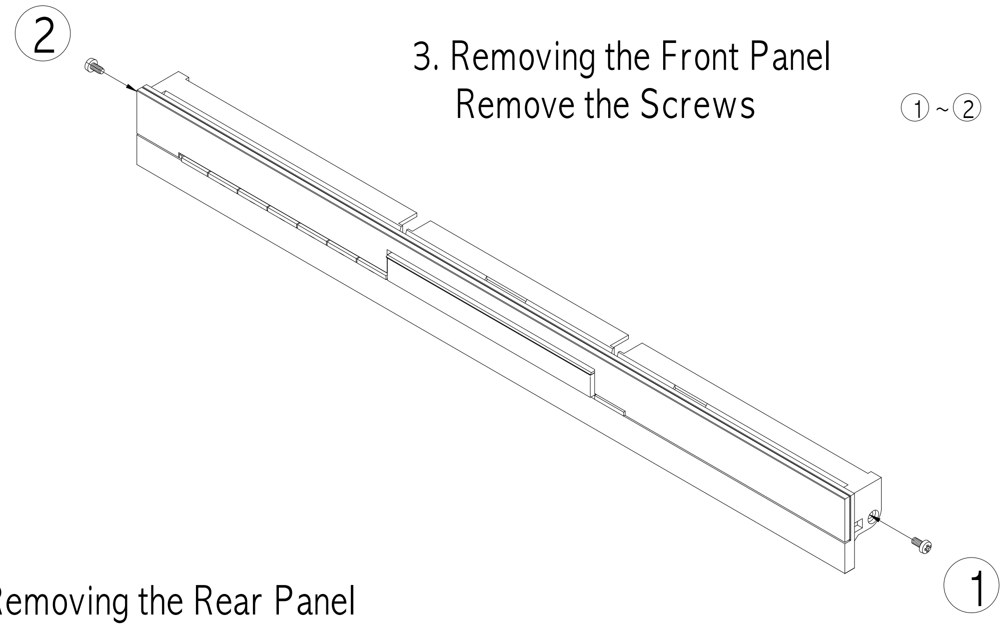
1. Removing the Top Cabinet
Remove the Screws ①~④



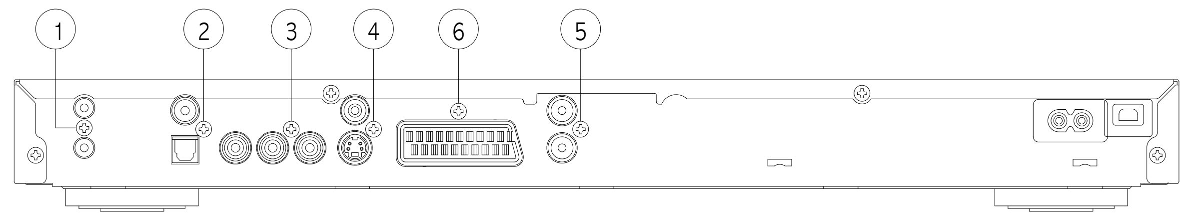
2. Removing the Bottom Chassis
Remove the Screws ①~②



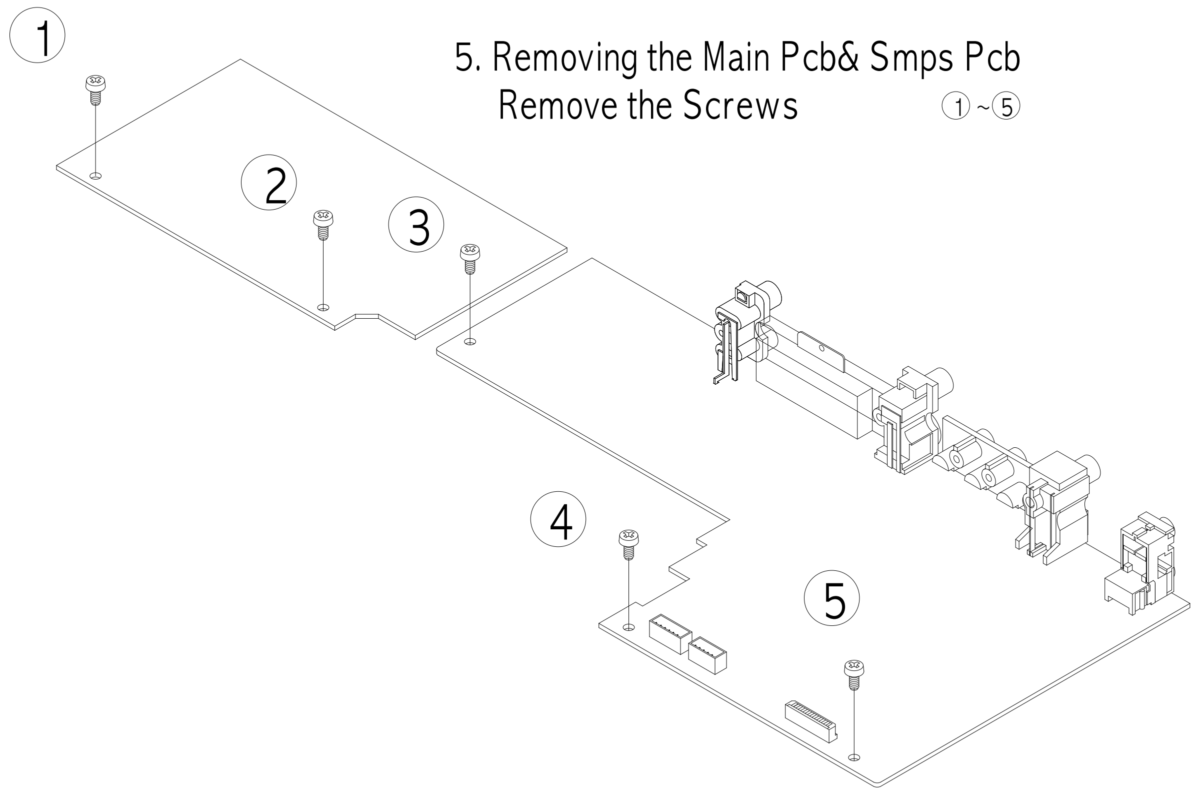
3. Removing the Front Panel
Remove the Screws ①~②



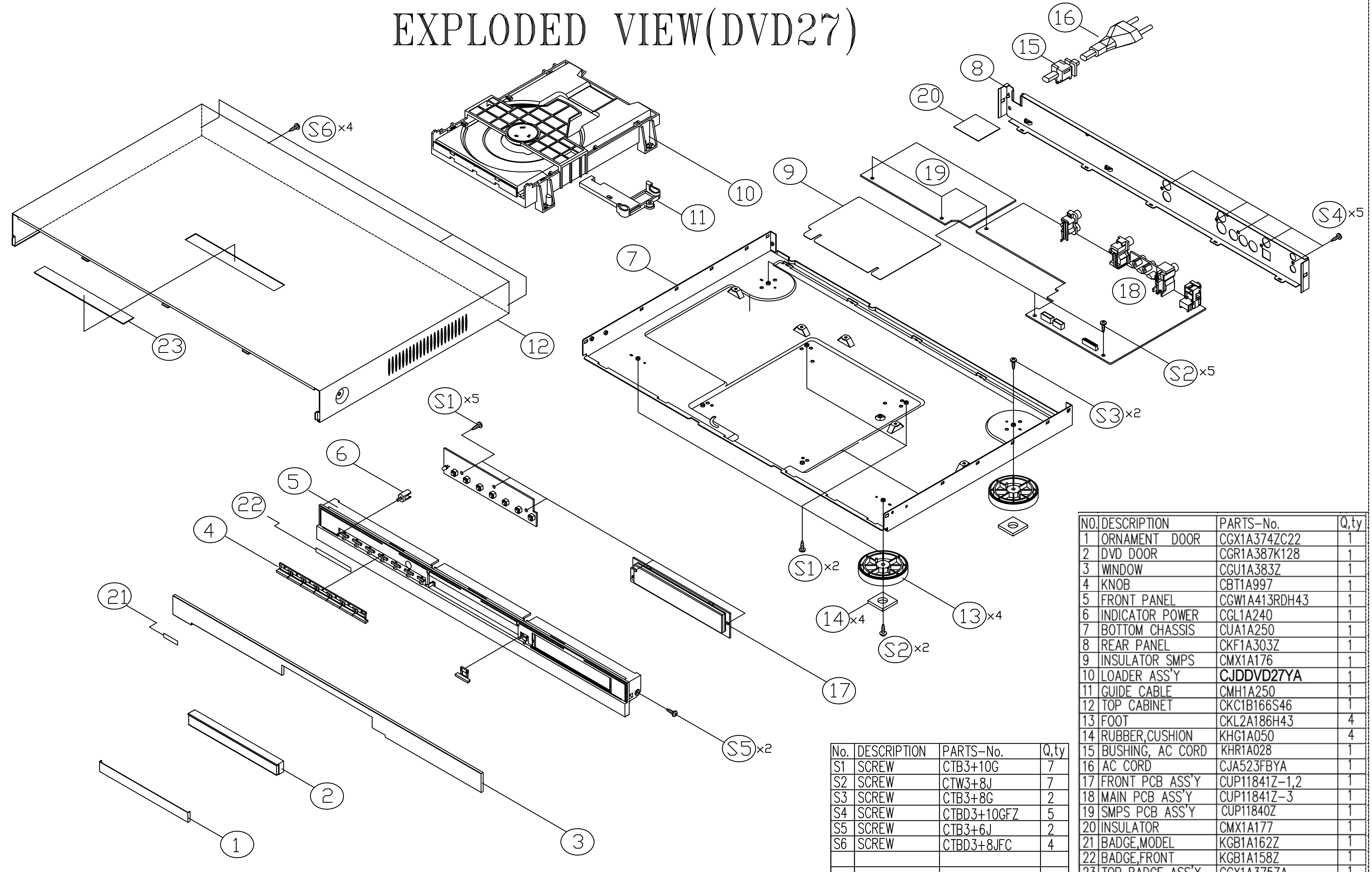
4. Removing the Rear Panel
Remove the Screws ①~⑥



5. Removing the Main Pcb& Smps Pcb
Remove the Screws ①~⑤



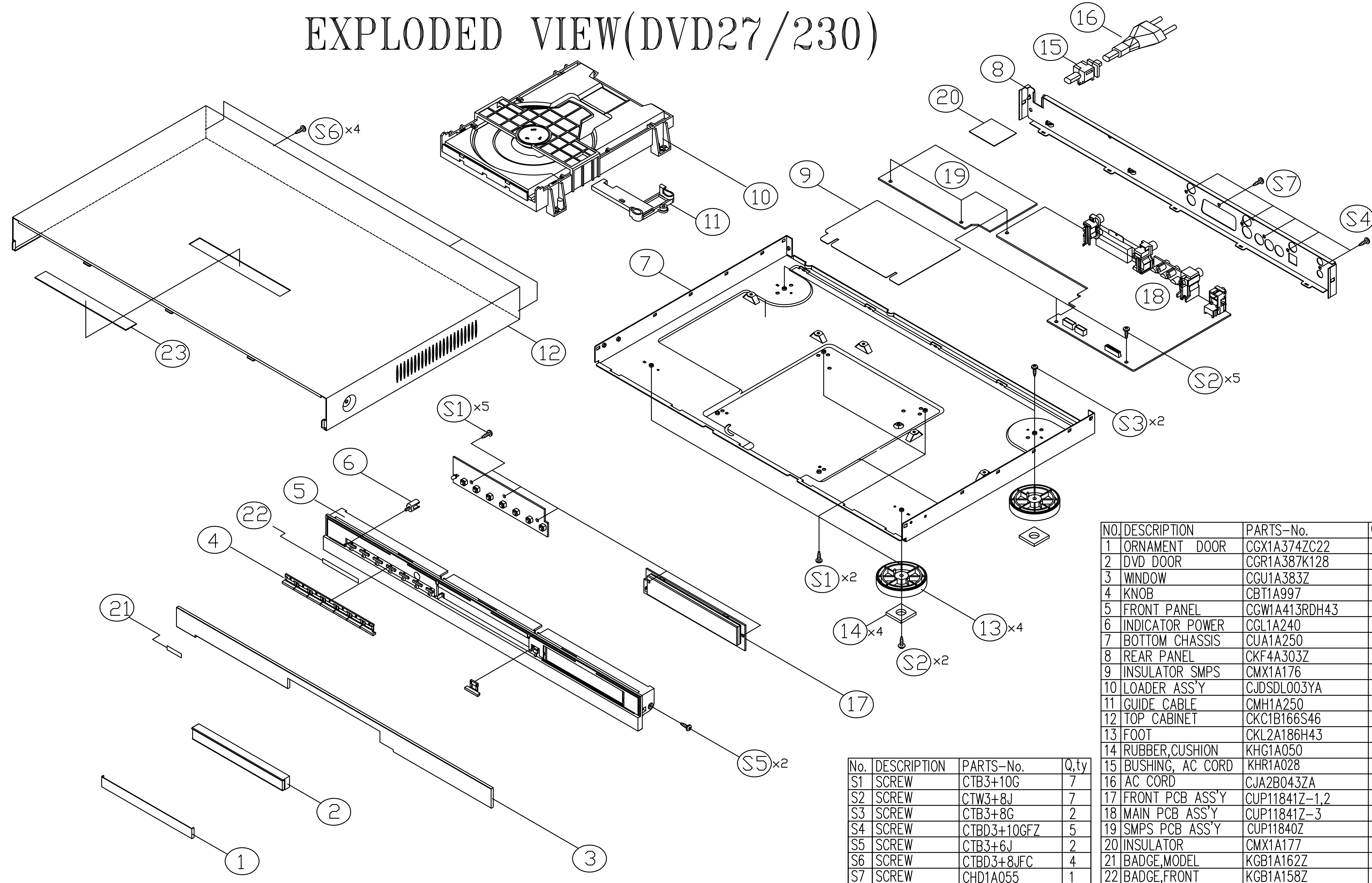
EXPLODED VIEW(DVD27)



NO.	DESCRIPTION	PARTS-No.	Q,ty
1	ORNAMENT DOOR	CGX1A374ZC22	1
2	DVD DOOR	CGR1A387K128	1
3	WINDOW	CGU1A383Z	1
4	KNOB	CBT1A997	1
5	FRONT PANEL	CGW1A413RDH43	1
6	INDICATOR POWER	CGL1A240	1
7	BOTTOM CHASSIS	CUA1A250	1
8	REAR PANEL	CKF1A303Z	1
9	INSULATOR SMPS	CMX1A176	1
10	LOADER ASS'Y	CJDDVD27YA	1
11	GUIDE CABLE	CMH1A250	1
12	TOP CABINET	CKC1B166S46	1
13	FOOT	CKL2A186H43	4
14	RUBBER,CUSHION	KHG1A050	4
15	BUSHING, AC CORD	KHR1A028	1
16	AC CORD	CJA523FBYA	1
17	FRONT PCB ASS'Y	CUP11841Z-1,2	1
18	MAIN PCB ASS'Y	CUP11841Z-3	1
19	SMPS PCB ASS'Y	CUP11840Z	1
20	INSULATOR	CMX1A177	1
21	BADGE,MODEL	KGB1A162Z	1
22	BADGE,FRONT	KGB1A158Z	1
23	TOP BADGE ASS'Y	CGX1A375ZA	1

No.	DESCRIPTION	PARTS-No.	Q,ty
S1	SCREW	CTB3+10G	7
S2	SCREW	CTW3+8J	7
S3	SCREW	CTB3+8G	2
S4	SCREW	CTBD3+10GFZ	5
S5	SCREW	CTB3+6J	2
S6	SCREW	CTBD3+8JFC	4

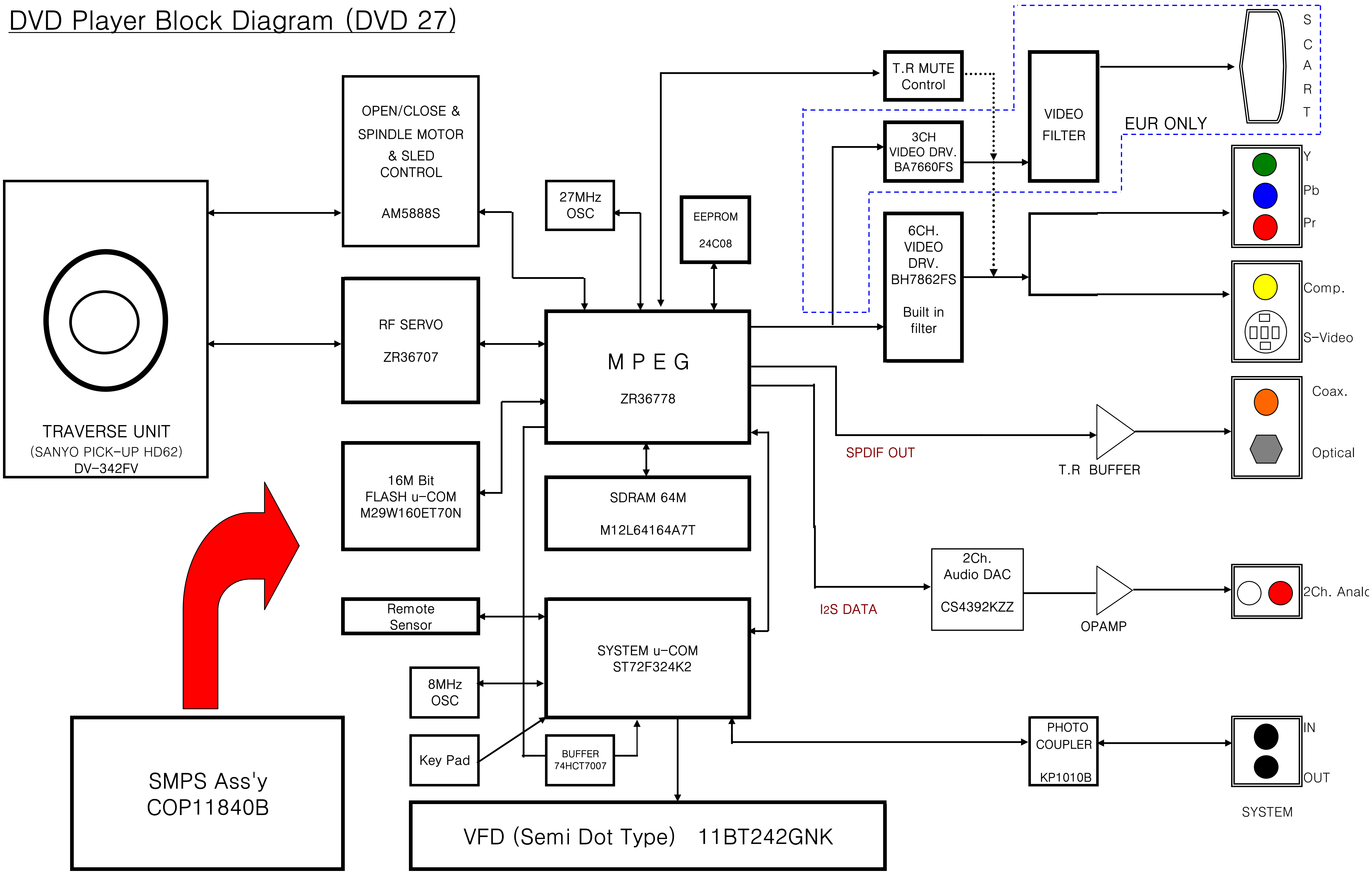
EXPLODED VIEW(DVD27/230)



No.	DESCRIPTION	PARTS-No.	Q,ty
S1	SCREW	CTB3+10G	7
S2	SCREW	CTW3+8J	7
S3	SCREW	CTB3+8G	2
S4	SCREW	CTBD3+10GFZ	5
S5	SCREW	CTB3+6J	2
S6	SCREW	CTBD3+8JFC	4
S7	SCREW	CHD1A055	1

NO.	DESCRIPTION	PARTS-No.	Q,ty
1	ORNAMENT DOOR	CGX1A374ZC22	1
2	DVD DOOR	CGR1A387K128	1
3	WINDOW	CGU1A383Z	1
4	KNOB	CBT1A997	1
5	FRONT PANEL	CGW1A413RDH43	1
6	INDICATOR POWER	CGL1A240	1
7	BOTTOM CHASSIS	CUA1A250	1
8	REAR PANEL	CKF4A303Z	1
9	INSULATOR SMPS	CMX1A176	1
10	LOADER ASS'Y	CJDSDL003YA	1
11	GUIDE CABLE	CMH1A250	1
12	TOP CABINET	CKC1B166S46	1
13	FOOT	CKL2A186H43	4
14	RUBBER,CUSHION	KHG1A050	4
15	BUSHING, AC CORD	KHR1A028	1
16	AC CORD	CJA2B043ZA	1
17	FRONT PCB ASS'Y	CUP11841Z-1,2	1
18	MAIN PCB ASS'Y	CUP11841Z-3	1
19	SMPS PCB ASS'Y	CUP11840Z	1
20	INSULATOR	CMX1A177	1
21	BADGE,MODEL	KGB1A162Z	1
22	BADGE,FRONT	KGB1A158Z	1
23	TOP BADGE ASS'Y	CGX1A375ZA	1

DVD Player Block Diagram (DVD 27)



DVD27 Electrical Parts List

Ref. Designator	Part Number	Description		Qty	
SMPS PCB ASS'Y					
Capacitors					
C905	CCKT1H104ZF	CAP , CERAMIC	50V 0.1UF	1	EA
C906	CCKT1H101KB	CAP , CERAMIC	100PF 50V KB	1	EA
C907	CCEA1HH100T	CAP , ELECT	10uF/50V	1	EA
C908	CCEA1HH470T	CAP , ELECT	47uF/50V	1	EA
C910	CCEA1HH1R0T	CAP , ELECT	1uF/50V	1	EA
C921	CCEA1EH331T	CAP , ELECT	330uF/25V	1	EA
C922	CCEA1HH0R1T	CAP , ELECT	0.1uF/50V	1	EA
C923	CCEA1EH331T	CAP , ELECT	330uF/25V	1	EA
C924	CCEA1VH101T	CAP , ELECT	100UF 50V	1	EA
C925	CCEA1EH331T	CAP , ELECT	330uF/50V	1	EA
C926	HCQI1H102JZT	CAP , MYLAR	1000PF 50V J	1	EA
C927	CCEA1HH470T	CAP , ELECT	47uF/50V	1	EA
C928	CCEA1HH470T	CAP , ELECT	47uF/50V	1	EA
C929	CCKT1H104ZF	CAP , CERAMIC	50V 0.1UF	1	EA
C931	CCKT1H104ZF	CAP , CERAMIC	50V 0.1UF	1	EA
C935	CCKT1H104ZF	CAP , CERAMIC	50V 0.1UF	1	EA
C901	HCQF2E104KZE	CAP , POLYPROPYLENE FILM	0.1uF/250V	1	EA
C902	HCQF2E104KZE	CAP , POLYPROPYLENE FILM	0.1uF/250V	1	EA
C903	CCET400VKRH470K	CAP , ELECT(400V/47uF)	KOSHIN KRH SERI	1	EA
C904	CCKT3A222KBL	CAP , CERAMIC	2200pF, 1KV DC	1	EA
C920	CCEA1EH102T	CAP , ELECT	1000uF/25V	1	EA
C930	CCKDHS222ME	CAP , CERAMIC (400V Y-CAP)	2200pF	1	EA
C932	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	1000pF	1	EA
C933	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	1000pF	1	EA
Semiconductors					
D906	HVDMTZJ12BT	DIODE , ZENER	12V 1/2W	1	EA
D907	HVD1N4148T	DIODE	1N4148	1	EA
D909	HVDMTZJ24BT	DIODE , ZENER	24V T77	1	EA
D910	HVD1N4148T	DIODE	1N4148	1	EA
D911	HVD1N4148T	DIODE	1N4148	1	EA
D912	HVDMTZJ5.1BT	DIODE , ZENER	5.1V, 1/2W	1	EA
D913		WIRE , COPPER	SN95/PB5 , 0.6		M
D925	HVD1N4148T	DIODE	1N4148	1	EA
D926	HVDMTZJ12BT	DIODE , ZENER	12V 1/2W	1	EA
D928	HVDMTZJ5.1BT	DIODE , ZENER	5.1V, 1/2W	1	EA
Q904	HVTKTC3198YT	TRANSISTOR	KTC3198Y	1	EA
Q905	HVTKTA1273YT	TR NORMAL KTA1273/PNP/TO-92L		1	EA
Q906	HVTKSC1008YT	TRANSISTOR	KSC1008Y	1	EA
Q907	HVTKRC102MT	TRANSISTOR	KRC102M	1	EA
Q908	HVTKRA102MT	TRANSISTOR	KRA102M	1	EA
Q909	HVTKSC1008YT	TRANSISTOR	KSC1008Y	1	EA
Q910	HVTKSC1008YT	TRANSISTOR	KSC1008Y	1	EA
Q912	HVDMCR100-6ZL1G	SCR (ON SEMI)	MCR100-6Z	1	EA
D901	HVD1N4007T	DIODE	1N4007	1	EA
D902	HVD1N4007T	DIODE	1N4007	1	EA

Ref. Designator	Part Number	Description		Qty	
SMPS PCB ASS'Y					
D903	HVD1N4007T	DIODE	1N4007	1	EA
D904	HVD1N4007T	DIODE	1N4007	1	EA
D905	HVDUF4007T	DIODE , SCHOTTKY	UF4007	1	EA
D908	HVD1N4007T	DIODE	1N4007	1	EA
D920	HVD31DQ06H	DIODE	31DQ06-FC5	1	EA
D921	HVDUF4007T	DIODE , SCHOTTKY	UF4007	1	EA
D922	HVD1N4937T	DIODE , RECTIFIERS	1N4937(600V/1A)	1	EA
D923	HVD1N4937T	DIODE , RECTIFIERS	1N4937(600V/1A)	1	EA
D924	HVDSF26T	DIODE , SUPER FAST	SF26	1	EA
IC91	BVISG6848DZ	IC,PWM	SG6848DZ	1	EA
Q901	BVICEF04N6	FET , CEF04N6	CEF04N6	1	EA
Q903	HVTKSB1151Y	TRANSISTOR	KSB1151Y	1	EA
PC91	HVIPC17L1CB	I.C , PHOTO COUPLER	PC17L1CB	1	EA
IC92	HVIKIA431BAT	I.C , REGULATOR	KIA431B	1	EA
Resistors					
R901	KROS1TJ105V	RES , METAL FILM (1/2W , 1M OHM)		1	EA
R903	CRD25TJ754T	RES	750KΩ, 1/4W	1	EA
R904	CRD25TJ754T	RES	750KΩ, 1/4W	1	EA
R905	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J	1	EA
R607	CRD25TJ123T	RES , CARBON	12KΩ, 1/4W	1	EA
R906	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1	EA
R907	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J	1	EA
R909	CRD20TJ100T	RES , CARBON	10 OHM 1/5W J	1	EA
R910	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J	1	EA
R911	CRD20TJ104T	RES , CARBON	100K OHM 1/5W J	1	EA
R912	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R913	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R914	CRD20TJ333T	RES , CARBON	33K OHM 1/5W J	1	EA
R920	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1	EA
R921	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J	1	EA
R607	CRD25TJ123T	RES , CARBON	12KΩ, 1/4W	1	EA
R922	CRD20TF3481T	RES , CARBON	3.48KΩ, 1/5W	1	EA
R923	CRD20TF3001T	RES , CARBON	3K 1/5W F	1	EA
R924	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1	EA
R925	CRD25TJ101T	RES , CARBON	100Ω, 1/4W	1	EA
R926	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1	EA
R928	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R929	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R930	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J	1	EA
R933	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R940	CRD20TJ472T	RES , CARBON	4.7K OHM 1/5W J	1	EA
R902	KRG1SANJ104H	RES,METAL OXIDE FILM	100KΩ, 1W	1	EA
R908	KRW1PJ1R5V	RES, WIRE WOUND	1W 1.5(J) NON-I	1	EA
R927	KRDS1TJ681V	RES , CARBON	680OHM 1/2W J	1	EA
Miscellaneous					
F901	KBA2C2000TLEY	FUSE	(2A/250V)	1	EA
T901	CLT9Z018ZE	TRANS (DVD 27)	EER2828H	1	EA
CN91	KJP02KA060ZY	WAFER	7.92MM(YUNHO)	1	EA

Ref. Designator	Part Number	Description		Qty	
SMPS PCB ASS'Y					
CN92	CJP12GA19ZY	WAFER		1	EA
FH91	KJCFC5S	HOLDER , FUSE		1	EA
FH92	KJCFC5S	HOLDER , FUSE		1	EA
L903	CLZ9Z040Z	COIL , CHOKE(6.8UH)	DR 6.5*7.5	1	EA
L905	CLZ9Z040Z	COIL , CHOKE(6.8UH)	DR 6.5*7.5	1	EA
NT91	KRT10D9MSFT	THERMISTER		1	EA
LF91	CLZ9Z060Y	LINE FILTER	CLZ9Z060Y	1	EA
	CVICEF04N6YA	FET. HEAT SINK ASS`Y	for Q901	1	EA
	CMY2A223	HEAT SINK		1	EA
	CTB3+8J	SCREW		1	EA
MAIN PCB ASS'Y					
Capacitors					
C100	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C101	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C102	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C103	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C104	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C106	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C115	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C117	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C120	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C122	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C146	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C156	HCUS1H330JA	CAP , CHIP	33pF / 50V DC	1	EA
C157	HCUS1H330JA	CAP , CHIP	33pF / 50V DC	1	EA
C158	HCUS1H330JA	CAP , CHIP	33pF / 50V DC	1	EA
C159	HCUS1H562KC	CAPACITOR	5600pF / 50V DC	1	EA
C160	HCUS1H562KC	CAPACITOR	5600pF / 50V DC	1	EA
C161	HCUS1H562KC	CAPACITOR	5600pF / 50V DC	1	EA
C162	HCUS1H561JA	CAP , CHIP	560pF / 50V DC	1	EA
C163	HCUS1H471JA	CAP , CHIP	470pF / 50V DC	1	EA
C164	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C165	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C166	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C167	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C168	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C169	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C170	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C172	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C173	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C174	HCUS1E333KC	CAP , CHIP	3300pF / 25V DC	1	EA
C175	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C176	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C178	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C179	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C180	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C181	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C183	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
C185	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C186	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C187	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C188	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C189	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C190	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C191	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C192	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C193	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C194	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C195	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C196	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C197	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C200	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C201	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C204	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C205	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C207	HCUS1H272KC	CAP , CHIP	2700pF / 50V DC	1	EA
C208	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C209	HCUS1H273KC	CAP,CERAMIC 0.027uF	ROHM 0.027UF	1	EA
C210	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C214	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C215	HCUS1H561JA	CAP , CHIP	560pF / 50V DC	1	EA
C217	HCUS1H273KC	CAP,CERAMIC 0.027uF	ROHM 0.027UF	1	EA
C218	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C220	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C222	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C225	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C227	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C228	HCUS1H222KC	CAP , CHIP	2200pF / 50V DC	1	EA
C229	HCUS1H222KC	CAP , CHIP	2200pF / 50V DC	1	EA
C230	HCUS1H222KC	CAP , CHIP	2200pF / 50V DC	1	EA
C231	HCUS1H222KC	CAP , CHIP	2200pF / 50V DC	1	EA
C232	HCUS1H330JA	CAP , CHIP	33pF / 50V DC	1	EA
C240	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C242	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C245	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C247	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C249	HCUS1H150JA	CAP CHIP	15pF / 50V DC	1	EA
C250	HCUS1H150JA	CAP CHIP	15pF / 50V DC	1	EA
C252	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C253	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C254	HCUS1H272KC	CAP , CHIP	2700pF / 50V DC	1	EA
C255	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C256	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C257	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C260	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C261	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C262	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C263	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C266	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
C267	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C277	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C281	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C282	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C283	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C284	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C285	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C295	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C303	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C304	HCSHB21A220B	CAP , TANTAL B2 SIZE	22uF / 10V	1	EA
C305	HCSHB21A220B	CAP , TANTAL B2 SIZE	22uF / 10V	1	EA
C306	HCSHB21A220B	CAP , TANTAL B2 SIZE	22uF / 10V	1	EA
C307	HCSHB21A220B	CAP , TANTAL B2 SIZE	22uF / 10V	1	EA
C308	HCSHB21A220B	CAP , TANTAL B2 SIZE	22uF / 10V	1	EA
C310	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C311	HCUS1H560JA	CAP , CHIP	56pF / 50V DC	1	EA
C312	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C313	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C336	HCUS1H682KB	CAP, CERAMIC, 1608 (PHILIPS)	6800pF / 50V DC	1	EA
C337	HCUS1H223KC	CAP , CHIP	0.022uF / 50V DC	1	EA
C338	HCUS1H221JA	CAP , CHIP	220pF / 50V DC	1	EA
C339	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C346	HCUS1H7R0DT	CAP, CHIP 1608	7pF / 50V DC	1	EA
C380	HCUS1H150JA	CAP CHIP	15pF / 50V DC	1	EA
C429	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C430	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
C431	HCUS1H221JA	CAP , CHIP	220pF / 50V DC	1	EA
C432	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C511	HCUS1H151JA	CAP , CHIP , 150PF JA	1608 SIZE	1	EA
C531	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C533	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C552	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C553	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C555	HCUS1H150JA	CAP CHIP	15pF / 50V DC	1	EA
C556	HCUS1H150JA	CAP CHIP	15pF / 50V DC	1	EA
C581	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C593	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C594	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C602	HCQI1H332JZT	CAP , MYLAR	3300PF 50V J	1	EA
C605	HCQI1H332JZT	CAP , MYLAR	3300PF 50V J	1	EA
C607	HCQI1H332JZT	CAP , MYLAR	3300PF 50V J	1	EA
C608	HCQI1H332JZT	CAP , MYLAR	3300PF 50V J	1	EA
C609	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C621	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C624	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C636	HCUS1H561JA	CAP , CHIP	560pF / 50V DC	1	EA
C637	HCUS1H561JA	CAP , CHIP	560pF / 50V DC	1	EA
C638	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C640	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C646	HCUS1H561JA	CAP , CHIP	560pF / 50V DC	1	EA
C647	HCUS1H561JA	CAP , CHIP	560pF / 50V DC	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
C663	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C809	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C810	HCUS1H510JA	CAP , CHIP , 51PF JA	1608 SIZE	1	EA
C822	HCUS1H510JA	CAP , CHIP , 51PF JA	1608 SIZE	1	EA
C823	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C828	HCUS1H220JA	CAP , CHIP	22pF / 50V DC	1	EA
C830	HCUS1H150JA	CAP CHIP	15pF / 50V DC	1	EA
C831	HCUS1H150JA	CAP CHIP	15pF / 50V DC	1	EA
C832	HCSHB21A220B	CAP , TANTAL B2 SIZE	22uF / 10V	1	EA
C834	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C881	HCUS1H150JA	CAP CHIP	15pF / 50V DC	1	EA
C105	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C116	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C118	CCEA1AH471T	CAP , ELECT	470UF 10V	1	EA
C119	CCEA1AH471T	CAP , ELECT	470UF 10V	1	EA
C121	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C137	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C155	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C177	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C182	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C184	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C202	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C203	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C206	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C213	CCEA1CH221T	CAP , ELECT	220uF / 16V	1	EA
C219	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C221	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C223	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C224	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C226	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C233	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C241	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C251	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C258	CCEA1HH4R7T	CAP , ELECT	4.7UF 50V	1	EA
C301	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C302	CCEA1CH221T	CAP , ELECT	220uF / 16V	1	EA
C433	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C504	CCEA1EH221T	CAP , ELECT	220UF 25V	1	EA
C508	CCEA1EH221T	CAP , ELECT	220UF 25V	1	EA
C510	CCEA1HH4R7T	CAP , ELECT	4.7UF 50V	1	EA
C530	CCEA1CH221T	CAP , ELECT	220uF / 16V	1	EA
C532	CCEA1CH221T	CAP , ELECT	220uF / 16V	1	EA
C548	CCEA1CH221T	CAP , ELECT	220uF / 16V	1	EA
C549	CCEA1CH221T	CAP , ELECT	220uF / 16V	1	EA
C561	CCEA1CH100T	CAP , ELECT	10pF / 16V	1	EA
C562	CCEA1HH1R0T	CAP , ELECT	1uF / 50V	1	EA
C582	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C620	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C623	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C648	CCEA1HH100T	CAP , ELECT	10uF / 50V	1	EA
C649	CCEA1HH100T	CAP , ELECT	10uF / 50V	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
C650	CCEA1HH100T	CAP , ELECT	10uF / 50V	1	EA
C651	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C652	CCEA1HH100T	CAP , ELECT	10uF / 50V	1	EA
C667	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C668	CCEA1CH100T	CAP , ELECT	10uF / 16V	1	EA
C669	CCEA1HH100T	CAP , ELECT	10uF / 50V	1	EA
C674	CCEA1CH100T	CAP , ELECT	10uF / 16V	1	EA
C675	CCEA1CH100T	CAP , ELECT	10uF / 16V	1	EA
C733	CCEA1HH3R3T	CAP , ELECT	3.3uF / 50V	1	EA
C795	CCEA1CH221T	CAP , ELECT	220pF / 16V	1	EA
C801	CCEA1AH331T	CAP , ELECT	330uF / 10V	1	EA
C802	CCEA1AH331T	CAP , ELECT	330uF / 10V	1	EA
C803	CCEA1CH220T	CAP , ELECT	220uF / 16V	1	EA
C804	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C805	CCEA0JH102T	CAP , ELECT	1000UF 6.3V	1	EA
C825	CCEA1HH100T	CAP , ELECT	10uF / 50V	1	EA
C826	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C827	CCEA1CH470T	CAP , ELECT	47UF 16V	1	EA
C829	CCEA1AH471T	CAP , ELECT	470UF 10V	1	EA
C835	CCEA1CH221T	CAP , ELECT	220uF / 16V	1	EA
C891	CCEA1AH471T	CAP , ELECT	470UF 10V	1	EA
Semiconductors					
D101	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D102	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D501	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D502	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D511	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D601	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D602	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D603	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D612	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D613	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
IC10	HVIZR36778	IC,MPEG (ZORAN)	ZR36778	1	EA
IC11	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V	1	EA
IC12	HVILM1117S-1V8	I.C , REGULATOR (1.8V)	LM1117-1V8	1	EA
IC15	HVIAT24C08N10SC	I.C, 8K EEPROM	AT24C08N10SC2.7	1	EA
IC20	HVITL3472IDR	IC,OP AMP 8-SOIC (TI)	TL3472IDR	1	EA
IC21	HVIM29W160ET70N 27	IC,16M FLASH (ST)	M29W160ET-70N6	1	EA
IC22	HVIM12L64164A7T	IC, 64M SDRAM (4X16)	M12L64164A7T	1	EA
IC23	HVIAM5888SLF	IC,Motor Driver(AMtek,Pb free)	AM5888S L/F	1	EA
IC24	HVIZR36707	IC,RF (ZORAN)	ZR36707	1	EA
IC41	BVIBH7862FS	IC , 6CH VIDEO DRIVER	ROHM (BH7862FS)	1	EA
IC43	HVICS4392KZZ	I.C , DAC	CS4392KZZ	1	EA
IC45	HVIST72F324K2 27	IC,FLASH (ST)	ST72F324K2	1	EA
IC47	HVITC74HCT7007F	I.C, HEX BUFFER	TC74HC7007AFEL	1	EA
IC51	HVILM1117S-5.0	IC REGULATOR/SOT-223	LM1117S-5.0	1	EA
IC52	HVINJM2068MDTE1	I.C , OP AMP	NJM2068MD-TE1	1	EA
Q105	HVTKTA1664YP	TRANSISTOR	KTA1664YP	1	EA
Q106	HVTKTA1664YP	TRANSISTOR	KTA1664YP	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
Q108	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1	EA
Q109	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1	EA
Q110	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1	EA
Q315	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q404	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1	EA
Q501	HVTKTA1504SYRTK	TRANSISTOR , CHIP	KTA1504S Y RTK	1	EA
Q502	HVTKTC3875SYRTK	TRANSISTOR , CHIP	KTC3875S Y RTK	1	EA
Q604	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q606	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q607	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q608	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q610	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q613	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q614	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q615	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q616	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q804	HVTKTA1504SYRTK	TRANSISTOR , CHIP	KTA1504S Y RTK	1	EA
Q805	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q806	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q821	HVTKTA1504SYRTK	TRANSISTOR , CHIP	KTA1504S Y RTK	1	EA
IC50	HVIKA79L08AZT	REGULATOR, -8V	KA79LXXAZTA	1	EA
Q605	HVTKSA916YT	TRANSISTOR	KSA916YT	1	EA
D103	KVD1N4003ST	DIODE	1N4003	1	EA
D104	KVD1N4003ST	DIODE	1N4003	1	EA
D105	KVD1N4003ST	DIODE	1N4003	1	EA
D106	KVD1N4003ST	DIODE	1N4003	1	EA
D112	HVDMTZJ30BT	DIODE , ZENER	30V, 1/2W	1	EA
IC46	BVIKP1010B	IC, PHOTO COUPLER	KP1010B	1	EA
IC49	HVIKIA7808API	REGULATOR, +8V	KIA7808 (KEC)	1	EA
Resistors					
R100	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R101	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%		1	EA
R102	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R103	CRJ10DJ330T	RES , CHIP	33Ω 1/10W	1	EA
R104	CRJ10DJ330T	RES , CHIP	33Ω 1/10W	1	EA
R106	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R112	CRJ10DJ202T	RES , CHIP	2kΩ 1/10W	1	EA
R113	CRJ10DJ202T	RES , CHIP	2kΩ 1/10W	1	EA
R114	CRJ10DJ121T	RES , CHIP	0Ω 1/10W	1	EA
R115	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R116	CRJ10DJ121T	RES , CHIP	120Ω 1/10W	1	EA
R117	CRJ10DJ121T	RES , CHIP	120Ω 1/10W	1	EA
R118	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R123	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R124	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R125	CRJ10DJ113T	RES, CHIP	11kΩ 1/10W	1	EA
R128	CRJ10DJ121T	RES , CHIP	120Ω 1/10W	1	EA
R133	CRJ10DF3920T	RES. CHIP (392R 1%)	1608 SIZE	1	EA
R134	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
R135	CRJ10DJ100T	RES , CHIP	10Ω 1/10W	1	EA
R136	CRJ10DJ221T	RES , CHIP	220Ω 1/10W	1	EA
R137	CRJ10DJ221T	RES , CHIP	220Ω 1/10W	1	EA
R138	CRJ10DJ100T	RES , CHIP	10Ω 1/10W	1	EA
R139	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R140	CRJ10DJ133T	RES , CHIP	13kΩ 1/10W	1	EA
R145	CRJ10DJ151T	RES, CHIP	150Ω 1/10W	1	EA
R146	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R147	CRJ10DJ104T	RES , CHIP	100kΩ 1/10W	1	EA
R148	CRJ10DJ151T	RES, CHIP	150Ω 1/10W	1	EA
R152	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R153	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R154	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R155	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R157	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R159	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R160	CRJ10DJ330T	RES , CHIP	33Ω 1/10W	1	EA
R162	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R163	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R164	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R165	CRJ10DJ330T	RES , CHIP	33Ω 1/10W	1	EA
R166	CRJ10DJ330T	RES , CHIP	33Ω 1/10W	1	EA
R167	CRJ10DJ330T	RES , CHIP	33Ω 1/10W	1	EA
R168	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R169	CRJ10DJ750T	RES , CHIP	75Ω 1/10W	1	EA
R170	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R171	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R172	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R173	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R174	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R175	CRJ10DJ912T	RES,CHIP(1/10W) 9.1K OHM J	9.1K OHM/1608	1	EA
R176	CRJ10DJ132T	RES , CHIP	1.3kΩ 1/10W	1	EA
R177	CRJ10DJ132T	RES , CHIP	1.3kΩ 1/10W	1	EA
R178	CRJ10DJ272T	RES , CHIP	2.7kΩ 1/10W	1	EA
R180	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R181	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R182	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R183	CRJ10DF1202T	RES, CHIP 1%	12kΩ 1/10W	1	EA
R184	CRJ10DJ471T	RES , CHIP	470Ω 1/10W	1	EA
R185	CRJ10DJ332T	RES , CHIP	3.3kΩ 1/10W	1	EA
R186	CRJ10DJ332T	RES , CHIP	3.3kΩ 1/10W	1	EA
R187	CRJ10DJ332T	RES , CHIP	3.3kΩ 1/10W	1	EA
R188	CRJ10DJ113T	RES, CHIP	11kΩ 1/10W	1	EA
R189	CRJ10DJ105T	RES , CHIP	1000kΩ 1/10W	1	EA
R190	CRJ10DJ223T	RES , CHIP	22kΩ 1/10W	1	EA
R191	CRJ10DJ223T	RES , CHIP	22kΩ 1/10W	1	EA
R192	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R193	CRJ10DJ332T	RES , CHIP	3.3kΩ 1/10W	1	EA
R195	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R201	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R202	CRJ10DJ622T	RES , CHIP	6.2kΩ 1/10W	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
R203	CRJ10DJ562T	RES , CHIP	5.6kΩ 1/10W	1	EA
R204	CRJ10DJ562T	RES , CHIP	5.6kΩ 1/10W	1	EA
R205	CRJ10DJ562T	RES , CHIP	5.6kΩ 1/10W	1	EA
R206	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R207	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%		1	EA
R209	CRJ10DF1002T	RES , CHIP	10K /1/10W/F	1	EA
R210	CRJ10DF1002T	RES , CHIP	10K /1/10W/F	1	EA
R211	CRJ10DF1002T	RES , CHIP	10K /1/10W/F	1	EA
R219	CRJ10DJ273T	RES , CHIP	27kΩ 1/10W	1	EA
R220	CRJ10DJ562T	RES , CHIP	5.6kΩ 1/10W	1	EA
R221	CRJ10DJ562T	RES , CHIP	5.6kΩ 1/10W	1	EA
R222	CRJ10DJ562T	RES , CHIP	5.6kΩ 1/10W	1	EA
R230	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R231	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R241	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM, 1%	1	EA
R243	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM, 1%	1	EA
R244	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM, 1%	1	EA
R265	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R284	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R285	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R287	CRJ10DJ113T	RES, CHIP	11kΩ 1/10W	1	EA
R301	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R302	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R377	CRJ10DJ221T	RES , CHIP	220Ω 1/10W	1	EA
R407	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R408	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R420	CRJ10DJ750T	RES , CHIP	75Ω 1/10W	1	EA
R421	CRJ10DJ680T	RES , CHIP	68Ω 1/10W	1	EA
R422	CRJ10DJ121T	RES , CHIP	120Ω 1/10W	1	EA
R423	CRJ10DJ820T	RES , CHIP	82Ω 1/10W	1	EA
R424	CRJ10DJ4R7T	RES , CHIP	4.7Ω 1/10W	1	EA
R431	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R432	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R433	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R434	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R435	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R436	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R503	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R504	CRJ10DJ473T	RES , CHIP	47kΩ 1/10W	1	EA
R505	CRJ10DJ470T	RES , CHIP	47Ω 1/10W	1	EA
R506	CRJ10DJ271T	RES , CHIP	270Ω 1/10W	1	EA
R511	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R512	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R513	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R514	CRJ10DJ100T	RES , CHIP	10Ω 1/10W	1	EA
R515	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R516	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R517	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R518	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R519	CRJ10DJ473T	RES , CHIP	47kΩ 1/10W	1	EA
R522	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
R533	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R544	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R549	CRJ10DJ104T	RES , CHIP	100kΩ 1/10W	1	EA
R552	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R553	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R561	CRJ10DJ473T	RES , CHIP	47kΩ 1/10W	1	EA
R564	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R593	CRJ10DJ330T	RES , CHIP	33Ω 1/10W	1	EA
R619	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R633	CRJ10DJ272T	RES , CHIP	2.7kΩ 1/10W	1	EA
R634	CRJ10DJ272T	RES , CHIP	2.7kΩ 1/10W	1	EA
R635	CRJ10DJ512T	RES , CHIP	5.1kΩ 1/10W	1	EA
R636	CRJ10DF4990T	RES, CHIP 499 OHM/1608/1%		1	EA
R637	CRJ10DF4990T	RES, CHIP 499 OHM/1608/1%		1	EA
R639	CRJ10DJ561T	RES , CHIP	560Ω 1/10W	1	EA
R640	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R641	CRJ10DJ224T	RES , CHIP	220kΩ 1/10W	1	EA
R642	CRJ10DJ224T	RES , CHIP	220kΩ 1/10W	1	EA
R643	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R644	CRJ10DJ272T	RES , CHIP	2.7kΩ 1/10W	1	EA
R645	CRJ10DJ272T	RES , CHIP	2.7kΩ 1/10W	1	EA
R646	CRJ10DJ152T	RES , CHIP	1.5kΩ 1/10W	1	EA
R647	CRJ10DJ152T	RES , CHIP	1.5kΩ 1/10W	1	EA
R649	CRJ10DJ561T	RES , CHIP	560Ω 1/10W	1	EA
R650	CRJ10DJ473T	RES , CHIP	47kΩ 1/10W	1	EA
R653	CRJ10DJ512T	RES , CHIP	5.1kΩ 1/10W	1	EA
R654	CRJ10DF4990T	RES, CHIP 499 OHM/1608/1%		1	EA
R655	CRJ10DF4990T	RES, CHIP 499 OHM/1608/1%		1	EA
R660	CRJ10DJ152T	RES , CHIP	1.5kΩ 1/10W	1	EA
R662	CRJ10DJ512T	RES , CHIP	5.1kΩ 1/10W	1	EA
R663	CRJ10DJ512T	RES , CHIP	5.1kΩ 1/10W	1	EA
R665	CRJ10DJ152T	RES , CHIP	1.5kΩ 1/10W	1	EA
R726	CRJ10DJ474T	RES, CHIP	470kΩ 1/10W	1	EA
R727	CRJ10DJ221T	RES , CHIP	220Ω 1/10W	1	EA
R728	CRJ10DJ223T	RES , CHIP	22kΩ 1/10W	1	EA
R729	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R730	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R733	CRJ10DJ222T	RES , CHIP	2.2kΩ 1/10W	1	EA
R734	CRJ10DJ222T	RES , CHIP	2.2kΩ 1/10W	1	EA
R739	CRJ10DJ224T	RES , CHIP	220kΩ 1/10W	1	EA
R740	CRJ10DJ224T	RES , CHIP	220kΩ 1/10W	1	EA
R801	CRJ10DJ820T	RES , CHIP	82Ω 1/10W	1	EA
R802	CRJ10DJ820T	RES , CHIP	82Ω 1/10W	1	EA
R803	CRJ10DJ820T	RES , CHIP	82Ω 1/10W	1	EA
R806	CRJ10DJ680T	RES , CHIP	68Ω 1/10W	1	EA
R816	CRJ10DJ390T	RES, CHIP	39Ω 1/10W	1	EA
R817	CRJ10DJ750T	RES , CHIP	75Ω 1/10W	1	EA
R818	CRJ10DJ750T	RES , CHIP	75Ω 1/10W	1	EA
R821	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R823	CRJ10DJ0R0T	RES , CHIP	0Ω 1/10W	1	EA
R824	CRJ10DJ680T	RES , CHIP	68Ω 1/10W	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
R825	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R826	CRJ10DJ222T	RES , CHIP	2.2kΩ 1/10W	1	EA
R827	CRJ10DJ221T	RES , CHIP	220Ω 1/10W	1	EA
R828	CRJ18AJ221T	RES , CHIP	220Ω 1/8W	1	EA
R829	CRJ10DJ104T	RES , CHIP	100kΩ 1/10W	1	EA
R830	CRJ10DJ390T	RES, CHIP	39Ω 1/10W	1	EA
R832	CRJ10DJ102T	RES , CHIP	1kΩ 1/10W	1	EA
R878	CRJ10DJ104T	RES , CHIP	100kΩ 1/10W	1	EA
R879	CRJ10DJ101T	RES , CHIP	100Ω 1/10W	1	EA
R895	CRJ10DJ221T	RES , CHIP	220Ω 1/10W	1	EA
R896	CRJ10DJ620T	RES , CHIP	62Ω 1/10W	1	EA
R673	CRD25TJ681T	RES , CARBON	680Ω 1/4W	1	EA
Miscellaneous					
CN11	KJP24GA195ZM	SMT FFC/FPC WAFER(0.5MM PITCH)	52559-2472 (PB	1	EA
L101	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L102	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L103	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L104	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L105	HLQ06E100KRZ	INDUCTOR , CHIP	3225 SIZE	1	EA
L106	HLQ06E100KRZ	INDUCTOR , CHIP	3225 SIZE	1	EA
L107	HLQ06E100KRZ	INDUCTOR , CHIP	3225 SIZE	1	EA
L109	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L110	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L111	HLZ9R006Z	BEAD , CHIP		1	EA
L112	HLZ9R006Z	BEAD , CHIP		1	EA
L113	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L114	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L115	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L116	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L117	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L120	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L121	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L518	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L519	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L520	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L522	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L523	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L611	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L612	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L613	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L801	HLQ08ER68KRZ	CHIP FERRITE INDUCTOR	2012-R68UH	1	EA
L804	HLQ09E8R2KRZ	CHIP , COIL		1	EA
L805	HLQ08ER68KRZ	CHIP FERRITE INDUCTOR	2012-R68UH	1	EA
L806	HLQ08ER39KRZ	CHIP FERRITE INDUCTOR	2012-R39UH	1	EA
L809	HLQ09E8R2KRZ	CHIP , COIL		1	EA
	CMD1A504	BRACKET , FIP		2	EA
BN01	CWB1C912060EN	WIRE ASS'Y		1	EA
CN03	CJP07GA01ZY	WAFER, STRAIGHT, 7PIN		1	EA
CN04	CJP15GA117ZY	WAFER , CARD CABLE		1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN PCB ASS'Y					
CN12	CJP05GA19ZY	WAFER, STRAIGHT, 5PIN		1	EA
CN13	CJP06GA19ZY	WAFER, STRAIGHT, 6PIN		1	EA
JK02	CJJ4N067Z	2P, JACK	RCA-201DAG-01	1	EA
JK03	CJJ4S043Z	JACK , BOARD		1	EA
JK04	CJJ9N003Z	JACK , (S-VIDEO+VHS)		1	EA
JK06	HJS9U008Z	Optical+Coaxial Jack (Gold Plate)	YKC22-0732N	1	EA
JK08	HJJ1D002Z	JACK, HOSIDEN	SR7400	1	EA
X101	HOX27000E180S	CRYSTAL , CHIP(27MHZ,SMD)	HC-49/US	1	EA
X501	HOX08000E160C	CRYSTAL		1	EA
	CTB3+10G	SCREW		2	EA
	CTB3+8G	SCREW		3	EA
	CTW3+8J	SCREW		7	EA
FRONT PCB					
Capacitors					
C401	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C402	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C403	HCUS1H102KC	CAP , CHIP	1000pF / 50V DC	1	EA
C405	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C406	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C408	HCUS1E104ZF	CAP , CHIP , 0.1UF ZF	1608 SIZE	1	EA
C404	CCEA1CKS470T	CAP , ELECT	47UF/16V	1	EA
Semiconductors					
IC60	HVIPT6315LQ	I.C VFD DRIVER	PT6315	1	EA
Q405	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q406	HVTKTA1504SYRTK	TRANSISTOR , CHIP	KTA1504S Y RTK	1	EA
Q407	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q408	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
D401	CVD50BOBBWGA	L.E.D , 2 COLOR (ORG , BLUE)	TOL-50BOBBWGA	1	EA
Resistors					
R409	CRJ10DJ100T	RES , CHIP	10Ω 1/10W	1	EA
R410	CRJ10DJ103T	RES , CHIP	10kΩ 1/10W	1	EA
R411	CRJ10DJ681T	RES, CHIP	680Ω 1/10W	1	EA
R412	CRJ10DJ681T	RES, CHIP	680Ω 1/10W	1	EA
R413	CRJ10DJ821T	RES, CHIP	820Ω 1/10W	1	EA
R414	CRJ10DJ122T	RES , CHIP	1.2kΩ 1/10W	1	EA
R415	CRJ10DJ152T	RES , CHIP	1.5kΩ 1/10W	1	EA
R416	CRJ10DJ222T	RES , CHIP	2.2kΩ 1/10W	1	EA
R417	CRJ10DJ332T	RES , CHIP	3.3kΩ 1/10W	1	EA
R418	CRJ10DJ472T	RES , CHIP	4.7kΩ 1/10W	1	EA
R419	CRJ10DJ221T	RES , CHIP	220Ω 1/10W	1	EA
R425	CRJ10DJ332T	RES , CHIP	3.3kΩ 1/10W	1	EA
R804	CRJ10DJ823T	RES , CHIP	82kΩ 1/10W	1	EA

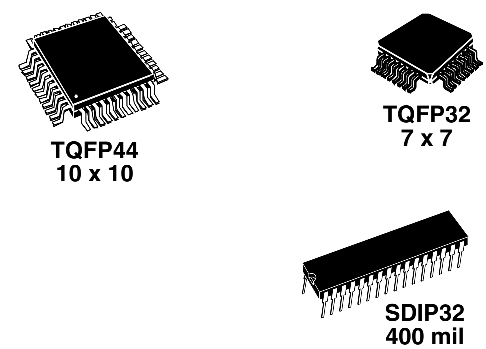
Ref. Designator	Part Number	Description		Qty	
FRONT PCB					
Miscellaneous					
IC61	HRVKSM603TH2	REMOCON SENSER CN	KSM-603TH2	1	EA
S401	HST1A020ZT	SW , TACT		1	EA
S402	HST1A020ZT	SW , TACT		1	EA
S403	HST1A020ZT	SW , TACT		1	EA
S404	HST1A020ZT	SW , TACT		1	EA
S405	HST1A020ZT	SW , TACT		1	EA
S406	HST1A020ZT	SW , TACT		1	EA
S407	HST1A020ZT	SW , TACT		1	EA
S408	HST1A020ZT	SW , TACT		1	EA
BN07	CWB1A906190EN	WIRE ASS'Y		1	EA
CN07	CJP06GA19ZY	WAFER, STRAIGHT, 6PIN		1	EA
CN05	CJP15GB113ZY	WAFER		1	EA
F401	HFL11BT242GNK	F.I.P	11-BT-242GNK (F	1	EA
MISCELLANEOUS/MECHANICAL					
	CUA1A259	CHASSSIS, BOTTOM		1	EA
	KHG1A050	RUBBER , CUSHION		4	EA
	KHG1A326Z	LUG CUSHION		2	EA
	KHR1A028	BUSHING , AC CORD		1	EA
	CHE154	CLAMPER , ARM			M
	CGWDVD27	FRONT PANEL ASS'Y		1	EA
	CBT1A997	KNOB, FUNCTION		1	EA
	CGL1A240	INDICATOR, POWER		1	EA
	CGR1A387K128	DOOR, DVD		1	EA
	CGUDVD27ZA	WINDOW ASS'Y		1	EA
	CGU1A383Z	WINDOW, FIP		1	EA
	KGB1A162Z	BADGE, DVD27		1	EA
	CGW1A413RDH43	PANEL, FRONT		1	EA
	CGX1A374ZC22	ORNAMENT, DOOR		1	EA
	CMZ1A105Z	FILTER, FIP		1	EA
	CTB3+10G	SCREW		5	EA
	CTB3+6J	SCREW		2	EA
	CWC1B2A15A160B	CABLE , CARD		1	EA
	KGB1A158Z	BADGE , HARMAN/KARDON(FRONT)		1	EA
	CGX1A375ZA	BADGE ASS'Y		1	EA
	CGX1A375M7G32	ORNAMENT , BADGE		1	EA
	CGX1A375ZA	BADGE , HARMAN/KARDON(TOP)		1	EA
	CKC1B166S46	TOP CABINET		1	EA
	CTBD3+10GFZ	SCREW , DOT		5	EA
	CTBD3+8JFC	SCREW , DOT		4	EA
	CUA1A250	BOTTOM CHASSIS ASS'Y		1	EA
	CHR301	CLAMPER		1	EA
	CJA523FBYA	CORD , POWER		1	EA
	CJDDVD27YA	MECHANISM ASS'Y		1	EA
	CJDDVD27YA	LOADER ASS'Y		1	EA
	CMH1A250	GUIDE, CABLE		1	EA
	CWB1B905150EE	WIRE ASS'Y		1	EA
	CWB5A906150SE	WIRE ASS'Y		1	EA

Ref. Designator	Part Number	Description		Qty	
MISCELLANEOUS/MECHANICAL					
	CWC1G2A24G250B	CARD CABLE (0.5mm Pitch, B Type)		1	EA
	CKF1A303Z	PANEL, REAR		1	EA
	CKL2A186H43	FOOT		4	EA
	CMX1A176	INSULATOR, SMPS		1	EA

ST72F324L, ST72324BL

3V RANGE 8-BIT MCU WITH 8 TO 32K FLASH/ROM, 10-BIT ADC, 4 TIMERS, SPI, SCI INTERFACE

- **Memories**
  - 8 to 32K dual voltage High Density Flash (HDFlash) or ROM with read-out protection capability. In-Application Programming and In-Circuit Programming for HDFlash devices
  - 384 to 1K bytes RAM
  - HDFlash endurance: 100 cycles, data retention: 20 years at 55°C
- **Clock, Reset And Supply Management**
  - Clock sources: crystal/ceramic resonator oscillators, internal RC oscillator, and bypass for external clock
  - PLL for 2x frequency multiplication
  - Four Power Saving Modes: Halt, Active-Halt, Wait and Slow
- **Interrupt Management**
  - Nested interrupt controller
  - 10 interrupt vectors plus TRAP and RESET
  - 9/6 external interrupt lines (on 4 vectors)
- **Up to 32 I/O Ports**
  - 32/24 multifunctional bidirectional I/O lines
  - 22/17 alternate function lines
  - 12/10 high sink outputs
- **4 Timers**
  - Main Clock Controller with: Real time base, Beep and Clock-out capabilities
  - Configurable watchdog timer
  - 16-bit Timer A with: 1 input capture, 1 output compare, external clock input, PWM and pulse generator modes
  - 16-bit Timer B with: 2 input captures, 2 output compares, PWM and pulse generator modes



- **2 Communication Interfaces**
  - SPI synchronous serial interface
  - SCI asynchronous serial interface
- **1 Analog Peripheral**
  - 10-bit ADC with up to 12 input ports
- **Instruction Set**
  - 8-bit Data Manipulation
  - 63 Basic Instructions
  - 17 main Addressing Modes
  - 8 x 8 Unsigned Multiply Instruction
- **Development Tools**
  - Full hardware/software development package
  - In-Circuit Testing capability

Device Summary

Features	ST72F324L(J/K)6	ST72F324L(J/K)4	ST72F324L(J/K)2	ST72324BL(J/K)4	ST72324BL(J/K)2
Program memory - bytes	Flash 32K	Flash 16K	Flash 8K	ROM 16K	ROM 8K
RAM (stack) - bytes	1024 (256)	512 (256)	384 (256)	512 (256)	384 (256)
Voltage Range	2.85 to 3.6V				
Temp. Range	up to -40°C to +85°C				
Packages	TQFP44 10x10, SDIP32, TQFP32 7x7				

Rev. 3

1 INTRODUCTION

The ST72F324L and ST72324BL devices are members of the ST7 microcontroller family designed for the 3V operating range. They can be grouped as follows:

– The 32-pin devices are designed for mid-range applications

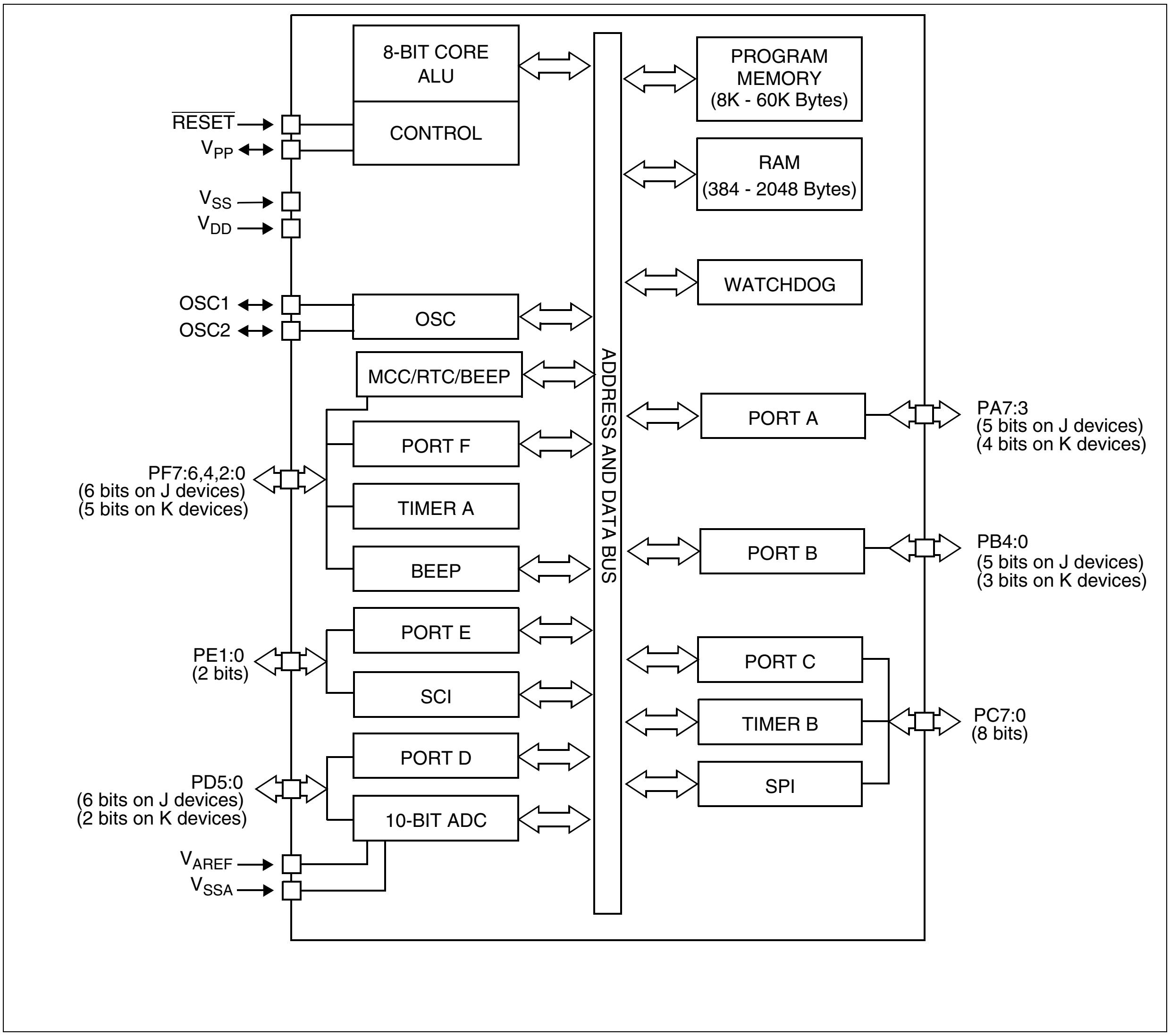
– The 44-pin devices target the same range of applications requiring more than 24 I/O ports.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with FLASH or ROM program memory.

Under software control, all devices can be placed in WAIT, SLOW, ACTIVE-HALT or HALT mode, reducing power consumption when the application is in idle or stand-by state.

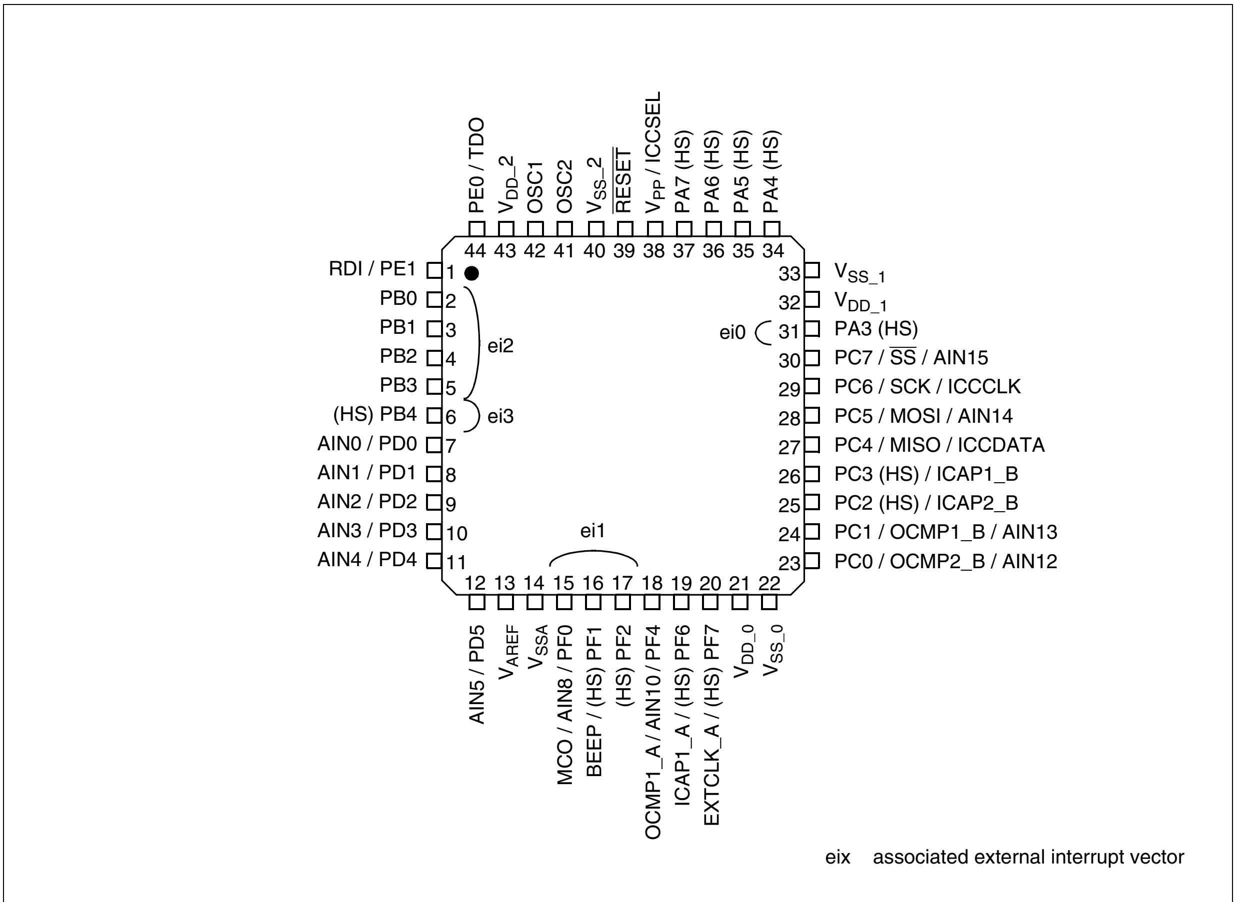
The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Figure 1. Device Block Diagram



2 PIN DESCRIPTION

Figure 2. 44-Pin TQFP Package Pinouts



ST72F324L, ST72324BL

PIN DESCRIPTION (Cont'd)

Figure 3. 32-Pin SDIP Package Pinout

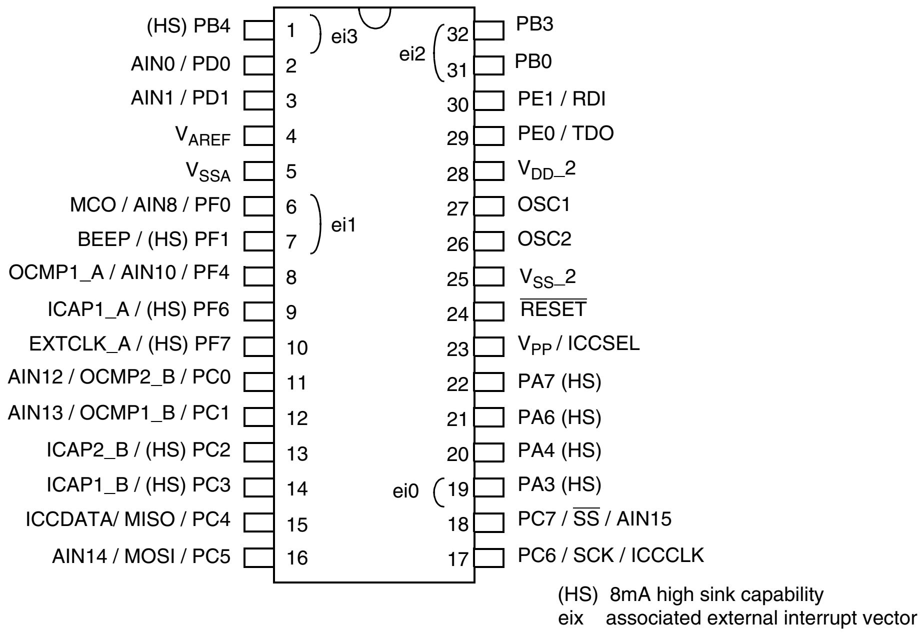
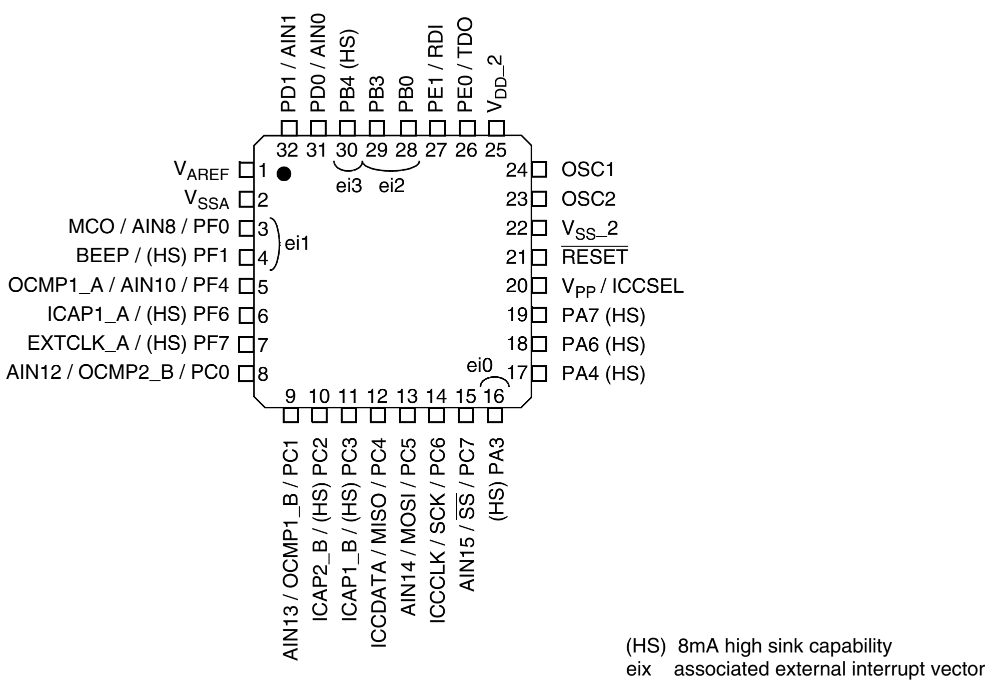


Figure 4. 32-Pin TQFP 7x7 Package Pinout



PIN DESCRIPTION (Cont'd)

For more details, refer to "ELECTRICAL CHARACTERISTICS" on page 110

Legend / Abbreviations for Table 1:

Type: I = input, O = output, S = supply

In/Output level: C = CMOS
C_T= CMOS with input trigger

Output level: HS = high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog ports
- Output: OD = open drain [2], PP = push-pull

Refer to "I/O PORTS" on page 39 for more details on the software configuration of the I/O ports.

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin n° TQFP44	Pin n° TQFP32	Pin n° SDIP32	Pin Name	Type	Level Input	Level Output	Port Input float	Port Input wpu	Port Input int	Port Input ana	Port Output OD	Port Output PP	Main function (after reset)	Alternate Function	
6	30	1	PB4 (HS)	I/O	C_T	HS	**X**	ei3			X	X	Port B4		
7	31	2	PD0/AIN0	I/O	C_T		**X**	X		X	X	X	Port D0	ADC Analog Input 0	
8	32	3	PD1/AIN1	I/O	C_T		**X**	X		X	X	X	Port D1	ADC Analog Input 1	
9			PD2/AIN2	I/O	C_T		**X**	X		X	X	X	Port D2	ADC Analog Input 2	
10			PD3/AIN3	I/O	C_T		**X**	X		X	X	X	Port D3	ADC Analog Input 3	
11			PD4/AIN4	I/O	C_T		**X**	X		X	X	X	Port D4	ADC Analog Input 4	
12			PD5/AIN5	I/O	C_T		**X**	X		X	X	X	Port D5	ADC Analog Input 5	
13	1	4	V_{AREF}	S									Analog Reference Voltage for ADC		
14	2	5	V_{SSA}	S									Analog Ground Voltage		
15	3	6	PF0/MCO/AIN8	I/O	C_T		**X**	ei1		X	X	X	Port F0	Main clock out (f_{OSC}/2)	ADC Analog Input 8
16	4	7	PF1 (HS)/BEEP	I/O	C_T	HS	**X**	ei1			X	X	Port F1	Beep signal output	
17			PF2 (HS)	I/O	C_T	HS	**X**		ei1		X	X	Port F2		
18	5	8	PF4/OCMP1_A/ AIN10	I/O	C_T		**X**	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
19	6	9	PF6 (HS)/ICAP1_A	I/O	C_T	HS	**X**	X			X	X	Port F6	Timer A Input Capture 1	
20	7	10	PF7 (HS)/ EXTCLK_A	I/O	C_T	HS	**X**	X			X	X	Port F7	Timer A External Clock Source	
21			V_{DD_0}	S									Digital Main Supply Voltage		
22			V_{SS_0}	S									Digital Ground Voltage		
23	8	11	PC0/OCMP2_B/ AIN12	I/O	C_T		**X**	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
24	9	12	PC1/OCMP1_B/ AIN13	I/O	C_T		**X**	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13

ST72F324L, ST72324BL

Pin n°			Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
							Input				Output				
TQFP44	TQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
25	10	13	PC2 (HS)/ICAP2_B	I/O	C_T	HS	X	X			X	X	Port C2	Timer B Input Capture 2	
26	11	14	PC3 (HS)/ICAP1_B	I/O	C_T	HS	X	X			X	X	Port C3	Timer B Input Capture 1	
27	12	15	PC4/MISO/ICCDA-TA	I/O	C_T		X	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
28	13	16	PC5/MOSI/AIN14	I/O	C_T		X	X		X	X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14
29	14	17	PC6/SCK/ICCCLK	I/O	C_T		X	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output
30	15	18	PC7/$\overline{SS}$/AIN15	I/O	C_T		X	X		X	X	X	Port C7	SPI Slave Select (active low)	ADC Analog Input 15
31	16	19	PA3 (HS)	I/O	C_T	HS	X		ei0		X	X	Port A3		
32			V_{DD_1}	S									Digital Main Supply Voltage		
33			V_{SS_1}	S									Digital Ground Voltage		
34	17	20	PA4 (HS)	I/O	C_T	HS	X	X			X	X	Port A4		
35			PA5 (HS)	I/O	C_T	HS	X	X			X	X	Port A5		
36	18	21	PA6 (HS)	I/O	C_T	HS	X				T		Port A6 [1)]		
37	19	22	PA7 (HS)	I/O	C_T	HS	X				T		Port A7 [1)]		
38	20	23	V_{PP} /ICCSEL	I									Must be tied low. In the flash programming mode, this pin acts as the programming voltage input V_{PP}. See Section 12.9.2 for more details. High voltage must not be applied to ROM devices.		
39	21	24	$\overline{RESET}$	I/O	C_T								Top priority non maskable interrupt.		
40	22	25	V_{SS_2}	S									Digital Ground Voltage		
41	23	26	OSC2	O									Resonator oscillator inverter output		
42	24	27	OSC1	I									External clock input or Resonator oscillator inverter input		
43	25	28	V_{DD_2}	S									Digital Main Supply Voltage		
44	26	29	PE0/TDO	I/O	C_T		X	X			X	X	Port E0	SCI Transmit Data Out	
1	27	30	PE1/RDI	I/O	C_T		X	X			X	X	Port E1	SCI Receive Data In	
2	28	31	PB0	I/O	C_T		X	ei2			X	X	Port B0		
3			PB1	I/O	C_T		X	ei2			X	X	Port B1		
4			PB2	I/O	C_T		X	ei2			X	X	Port B2		
5	29	32	PB3	I/O	C_T		X		ei2		X	X	Port B3		

Notes:

1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

2. In the open drain output column, “T” defines a true open drain I/O (P-Buffer and protection diode to V_{DD}

are not implemented). See See "I/O PORTS" on page 39. and Section 12.8 I/O PORT PIN CHARACTERISTICS for more details.

3. OSC1 and OSC2 pins connect a crystal/ceramic resonator, or an external source to the on-chip oscillator; see Section 1 INTRODUCTION and Section 12.5 CLOCK AND TIMING CHARACTERISTICS for more details.

4. On the chip, each I/O port has 8 pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption.

M29W160ET
M29W160EB

16 Mbit (2Mb x8 or 1Mb x16, Boot Block) 3V Supply Flash Memory

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V for Program, Erase and Read
- ACCESS TIMES: 70, 90ns
- PROGRAMMING TIME
  - 10µs per Byte/Word typical
- 35 MEMORY BLOCKS
  - 1 Boot Block (Top or Bottom Location)
  - 2 Parameter and 32 Main Blocks
- PROGRAM/ERASE CONTROLLER
  - Embedded Byte/Word Program algorithms
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code M29W160ET: 22C4h
  - Bottom Device Code M29W160EB: 2249h

Figure 1. Packages



SUMMARY DESCRIPTION

The M29W160E is a 16 Mbit (2Mb x8 or 1Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged, see Figures 5 and 6, Block Addresses. The first or last 64 KBytes have been divided into four additional blocks. The 16 KByte Boot Block can be used for small initialization code to start the microprocessor, the two 8 KByte Parameter Blocks can be used for parameter storage and the remaining 32K is a small Main Block where the application may be stored.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered TSOP48 (12 x 20mm) and TFBGA48 (0.8mm pitch) packages. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

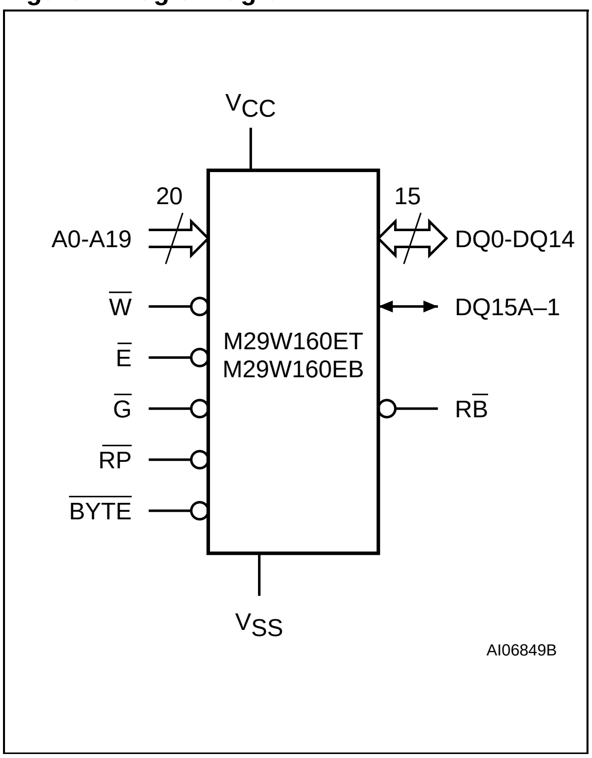


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
R$\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

M29W160ET, M29W160EB

Figure 3. TSOP Connections

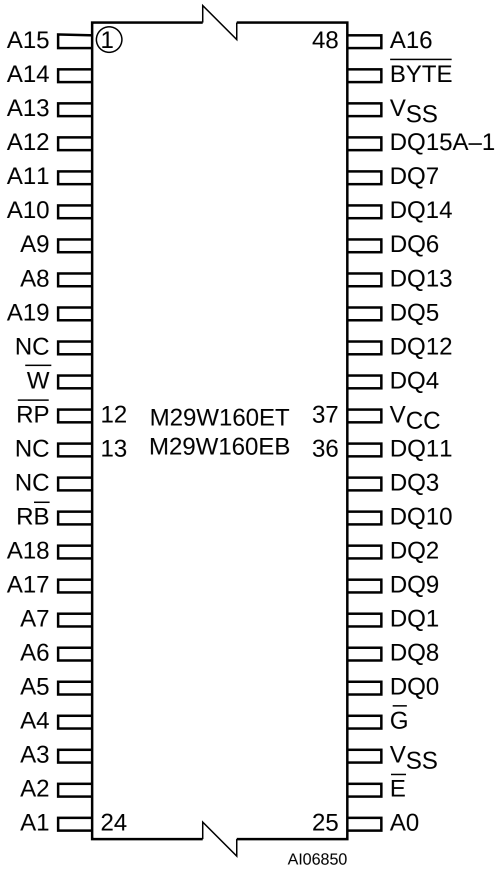
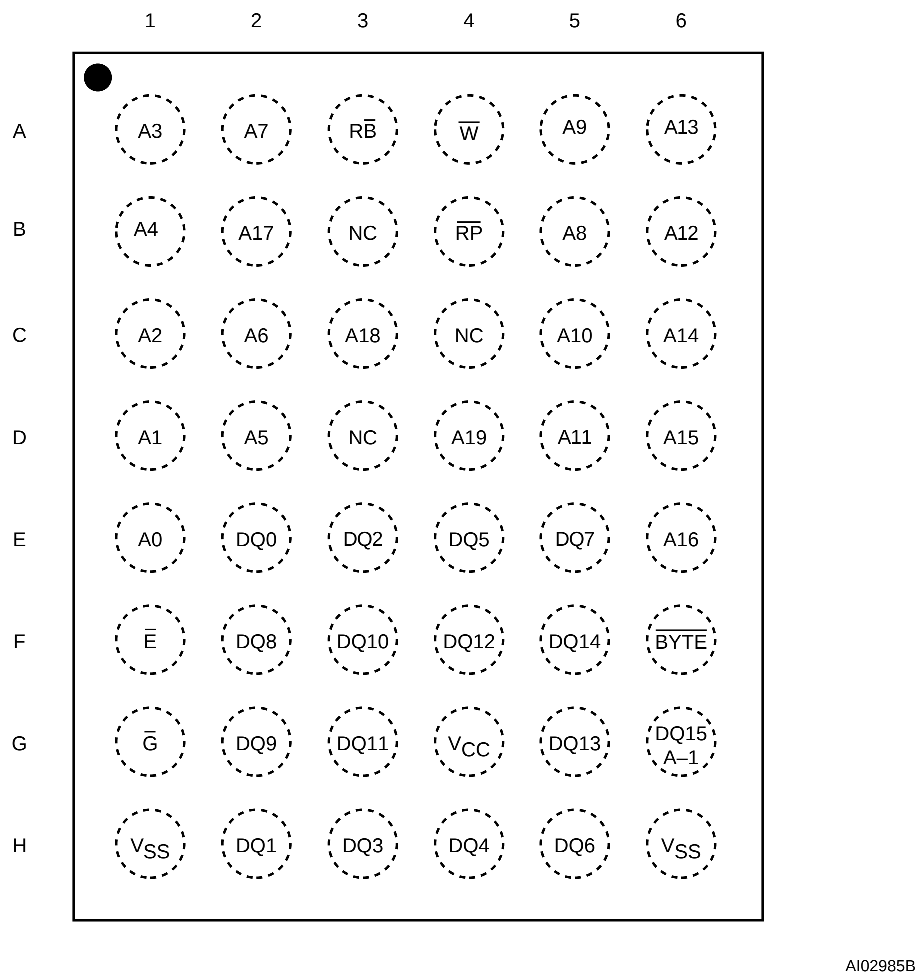


Figure 4. TFBGA Connections (Top view through package)



ESMT **M12L64164A**

SDRAM 1M x 16 Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

ORDERING INFORMATION

54 Pin TSOP (Type II)
(400mil x 875mil)

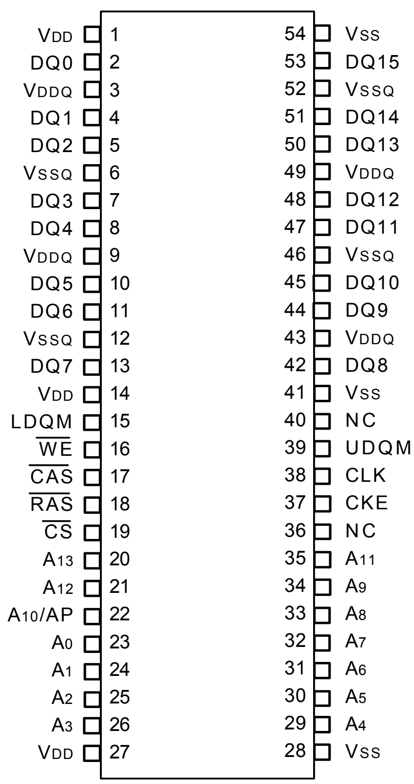
PRODUCT NO.	MAX FREQ.	PACKAGE
M12L64164A-6T	166MHz	TSOP II
M12L64164A-7T	143MHz	

GENERAL DESCRIPTION

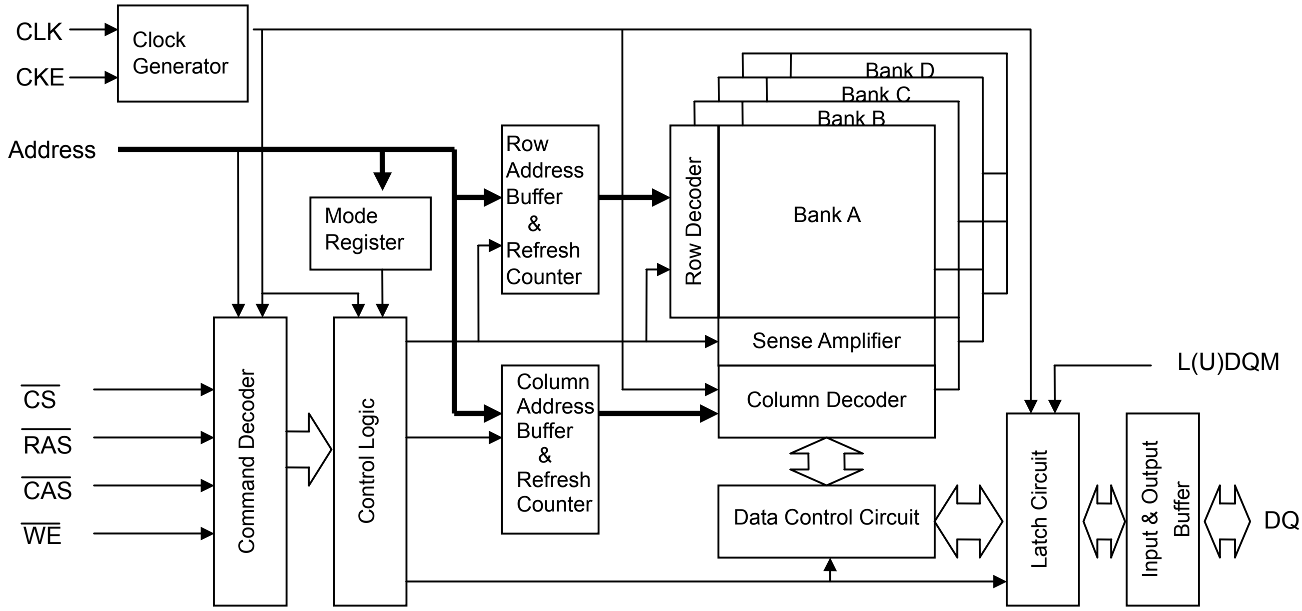
The M12L64164A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits. Synchronous design allows precise cycle controls with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

PIN ASSIGNMENT

Top View



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
A12 , A13	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

ESMT **M12L64164A**

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A13 A12	A10/AP	A11 A9~A0	Note
Register	Mode Register set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry	H	L	L	L	L	H	X	X			3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operating Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V = Valid , X = Don't Care. H = Logic High , L = Logic Low)

Note : 1.OP Code : Operating Code
A0~A11 & A13~A12 : Program keys. (@ MRS)
2.MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3.Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge of command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4.A13~A12 : Bank select addresses.
If both A13 and A12 are "Low" at read ,write , row active and precharge ,bank A is selected.
If both A13 is "Low" and A12 is "High" at read ,write , row active and precharge ,bank B is selected.
If both A13 is "High" and A12 is "Low" at read ,write , row active and precharge ,bank C is selected.
If both A13 and A12 are "High" at read ,write , row active and precharge ,bank D is selected
If A10/AP is "High" at row precharge , A13 and A12 is ignored and all banks are selected.
5.During burst read or write with auto precharge. new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.
6.Burst stop command is valid at every burst length.
7.DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after.(Read DQM latency is 2)

ESMT M12L64164A

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A13~A12	A11~A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	RFU	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	**A7**	**Type**	**A6**	**A5**	**A4**	**Latency**	**A3**	**Type**	**A2**	**A1**	**A0**	**BT = 0**	**BT = 1**
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
			1	0	0	Reserved			1	0	0	Reserved	Reserved
			1	0	1	Reserved			1	0	1	Reserved	Reserved
			1	1	0	Reserved			1	1	0	Reserved	Reserved
			1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : 256

POWER UP SEQUENCE

1.Apply power and start clock, Attempt to maintain CKE = ”H”, DQM = ”H” and the other pin are NOP condition at the inputs.
2. Maintain stable power , stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue mode register set command to initialize the mode register.
cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. RFU(Reserved for future use) should stay “0” during MRS cycle.

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE(CKE)

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + t_{SS}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (A13~A12)

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The A13~A12 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The banks addressed A13~A12 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0~A11)

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 12 address input pins (A0~A11). The 12 row addresses are latched along with $\overline{RAS}$ and A13~A12 during bank active command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and A13~A12 during read or with command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, The SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

   The device is now ready for normal operation.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A11 and A13~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field uses A0~A2, burst type uses A3, CAS latency (read latency from column address) use A4~A6, vendor specific options or test mode use A7~A8, A10/AP~A11 and A13~A12. The write burst length is programmed using A9. A7~A8, A10/AP~A11 and A13~A12 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

DEVICE OPERATIONS (Continued)

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of $t_{RCD\ (min)}$ from the time of bank activation. t_{RCD} is the internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing $t_{RCD\ (min)}$ with cycle time of the clock and then rounding of the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. $t_{RRD\ (min)}$ specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by $t_{RAS\ (min)}$. Every SDRAM bank activate command must satisfy $t_{RAS\ (min)}$ specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by $t_{RAS\ (max)}$ and $t_{RAS\ (max)}$ can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least $t_{RCD\ (min)}$ before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be complete by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used mask input and output operations. It works similar to $\overline{OE}$ during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge is performed on an active bank by asserting low on clock cycles required between bank activate and clock cycles required between bank activate and $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid A13~A12 of the bank to be procharged. The precharge command can be asserted anytime after $t_{RAS\ (min)}$ is satisfy from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing tRP with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by $t_{RAS\ (max)}$. Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to power-down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

DEVICE OPERATIONS (Continued)

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy $t_{RAS\ (min)}$ and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst write by asserting high on A10/AP, the bank is precharge command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A10/AP after all banks have satisfied $t_{RAS\ (min)}$ requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge all, all banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by $t_{RFC\ (min)}$. The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or the burst of 4096 auto refresh cycles in 64ms.

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption. The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the refresh.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

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FUNCTION TURTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (&Bank) Active ; Latch RA	
	L	L	H	L	BA	A10/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	Term burst → Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	Term burst → Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	3
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	

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Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
Read with Auto Precharge	H	X	X	X	X	X	NOP → Idle after tRP	
	L	H	H	H	X	X	NOP → Idle after tRP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	NOP → Idle after tRPL	4
	L	L	L	X	X	X	ILLEGAL	
Row Activating	H	X	X	X	X	X	NOP → Row Active after tRCD	
	L	H	H	H	X	X	NOP → Row Active after tRCD	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP → Idle after tRFC	
	L	H	H	X	X	X	NOP → Idle after tRFC	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP → Idle after 2clocks	
	L	H	H	H	X	X	NOP → Idle after 2clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations : RA = Row Address BA = Bank Address
NOP = No Operation Command CA = Column Address AP = Auto Precharge

*Note : 1. All entries assume the CKE was active (High) during the precharge clock and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of the bnak.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharge or in idle state. May precharge bank indicated by BA (and A10/AP).
5. Illegal if any bank is not idle.

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FUNCTION TRUTH TABLE (TABLE2)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh → Idle after tRFC (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh → Idle after tRFC (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh → ABI	7
	L	H	L	H	H	H	X	Exit Self Refresh → ABI	7
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table1	
	H	L	H	X	X	X	X	Enter Power Down	8
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	H	H	X	NOP	
	H	L	L	L	L	L	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Abbreviations **:** ABI = All Banks Idle, RA = Row Address

*Note : 6.CKE low to high transition is asynchronous.
7.CKE low to high transition is asynchronous if restart internal clock.
A minimum setup time 1CLK + t_{SS} must be satisfy before any command other than exit.
8.Power down and self refresh can be entered only from the all banks idle state.
9.Must be a legal command.

Multimedia ICs

High-performance 6-channel video driver IC for progressive DVD

BH7862FS

BH7862FS is a 6-channel video driver IC developed for progressive DVD player/recorder. Special filters adjusted to each band of various video signals are incorporated into a single chip. Extended definition, size reduction, and high cost performance can be achieved in DVD players.

●Application

DVD players, DVD recorders

●Features

1) Each high-performance filter, 6dB amplifier, and 75Ω driver for DVD are incorporated into a single chip.
2) Driver 6ch (Y, C, MIX, and PY, Pb, Pr for progressive)
3) Group delay difference between chroma signal and luminance signal is a small number of nsec.
4) Drive 2 lines of each signal
5) Operating by 5V single power supply
6) Built-in mute circuit

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Impressed voltage	V_{CC} max	6.0	V
Power dissipation	Pd	0.95*	W
Operating temperature range	Topr	−10~+70	°C
Storage temperature range	Tstg	−55~+150	°C

* Reduced by −7.6mW for each increase in Ta of 1°C over 25°C.
PCB (70mm×70mm, t=1.6mm) glass epoxy mounting.

●Recommended operating conditions (Ta = 25°C)

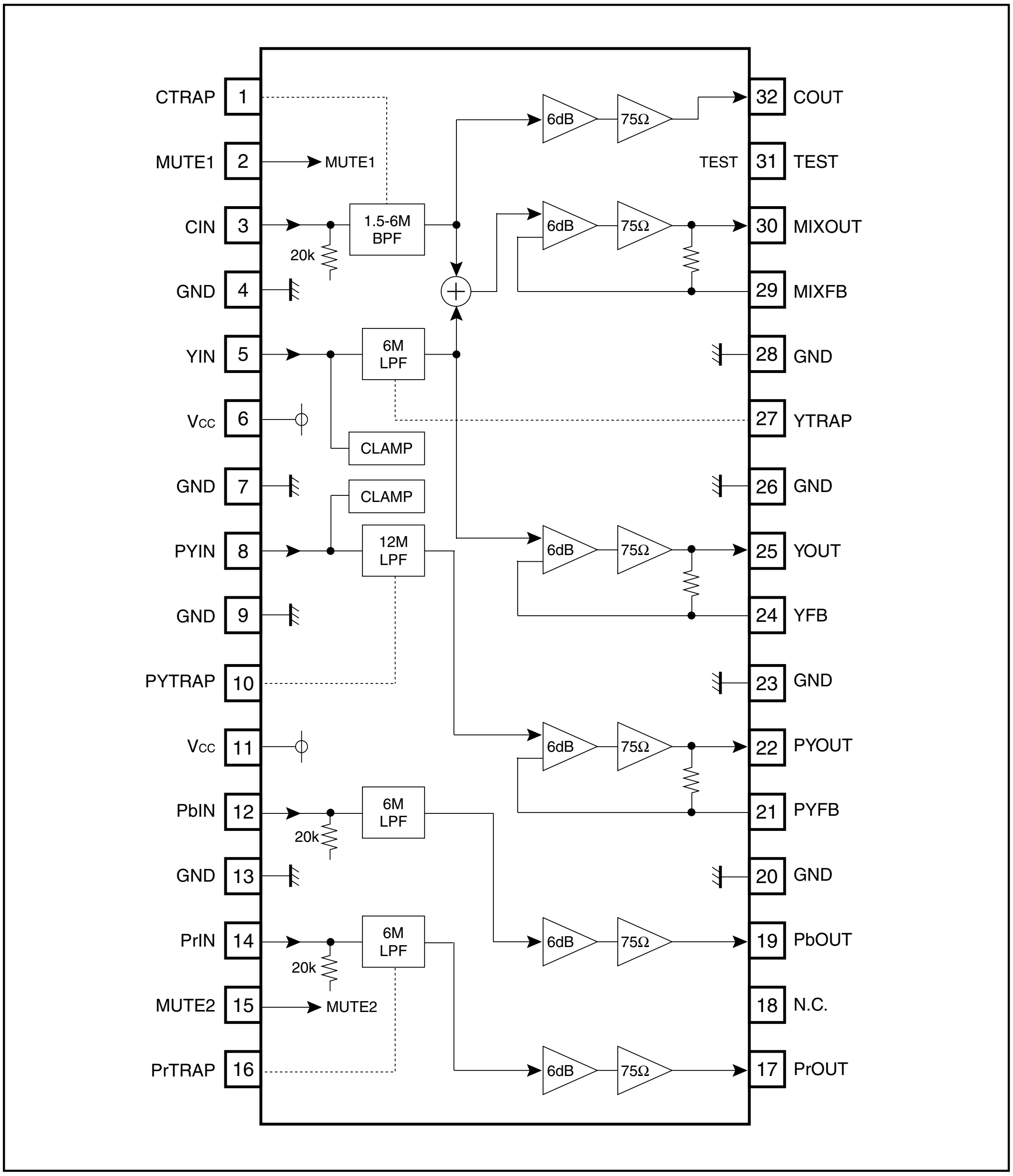
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	−	5.5	V

◎Radiation resistance is not included in the design.

BH7862FS

Multimedia ICs

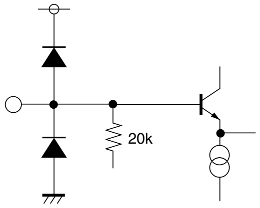
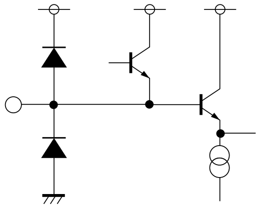
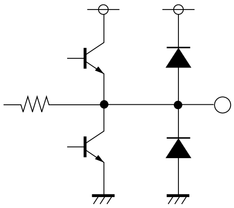
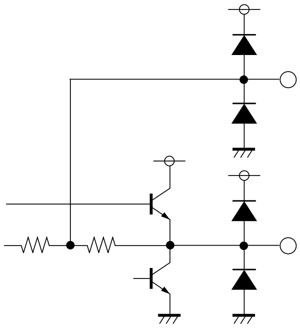
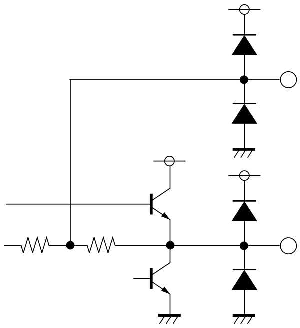
●Block diagram



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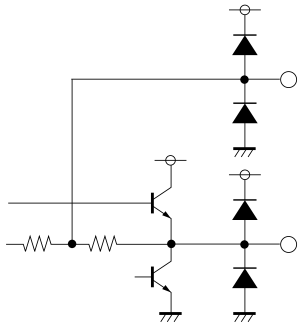
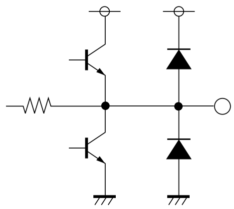
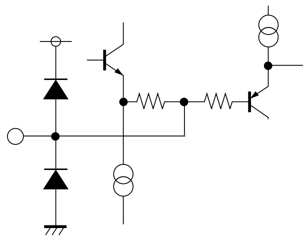
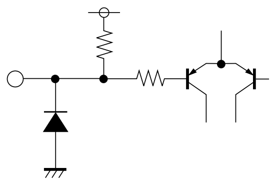
Multimedia ICs

●Pin descriptions and Input / output circuits

Pin No.	Pin name	Input/output equivalent circuit	Pin description
3 12 14	CIN PbIN PrIN		Signal input terminal. Input terminal for chroma signal and color-difference signal. Bias type input. The input impedance is 20kΩ.
5 8	YIN PYIN		Signal input terminal. Input terminal for luminance signal. Di clamp input.
32	COUT		Signal output terminal. Output terminal for chroma signal.
29 30	MIXFB MIXOUT		Signal output terminal. Output terminal for Y/C MIX signal.
24 25	YFB YOUT		Signal output terminal. Output terminal for luminance signal (interlaced type).

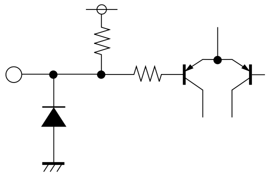
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Multimedia ICs

Pin No.	Pin name	Input/output equivalent circuit	Pin description
21 22	PYFB PYOUT		Signal output terminal. Output terminal for luminance signal (progressive type).
17 19	PrOUT PbOUT		Signal output terminal. Output terminal for color-difference signal.
1 27 10 16	CTPAP YTRAP PYTRAP PrTRAP		Terminal for LC resonance.
6 11	Vcc		Power supply voltage. Vcc is separated into 6 pin and 11 pin. That is to say, C, MIX and Y are partitioned by 6 pin and PY, Pb and Pr by 11 pin. They and not connected internally. Connect them externally when using.
4 7 9 13 20 23 26 28	GND		Grounding terminal.
2	MUTE1		Mute control terminal. C, MIX and Y are muted simultaneously by setting MUTE to "L".

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Multimedia ICs

Pin No.	Pin name	Input/output equivalent circuit	Pin description
12	MUTE2		Mute control terminal. PY, Pb and PR are muted simultaneously by setting MUTE to "L".
31	TEST		Test terminal. Usually, short-circuit this terminal to GND when using it.
18	N.C.		–

3-channel 75Ω driver
BA7660FS

The BA7660FS is a 75Ω driver with a 6dB amplifier and three internal circuits, and provides 75Ω drive of composite Y signals and C signals, as well as RGB signals. Each load is capable of driving two circuits, and a sag correction function reduces the capacitance of the output coupling capacitor.
The input voltage is within a range of 0V to 1.5V, enabling direct connection of ordinary D / A converter output. An internal power-saving circuit is also included which provides simultaneous muting on all three channels, and output pin shorting protection.

●Applications
DVDs, set top boxes and other digital video devices

●Features
1) Can be coupled directly to D / A converter output.
2) Operates at a low power consumption (115mW typ.).
3) Internal output muting circuit.
4) Internal power-saving circuit.
5) Internal output protection circuit.
6) An internal sag correction function makes it possible to reduce the capacitance of the output coupling capacitor.
7) Each load is capable of driving two circuits.
8) The compact 16-pin SSOP-A package is used.

●Absolute maximum ratings (Ta = 25°C)

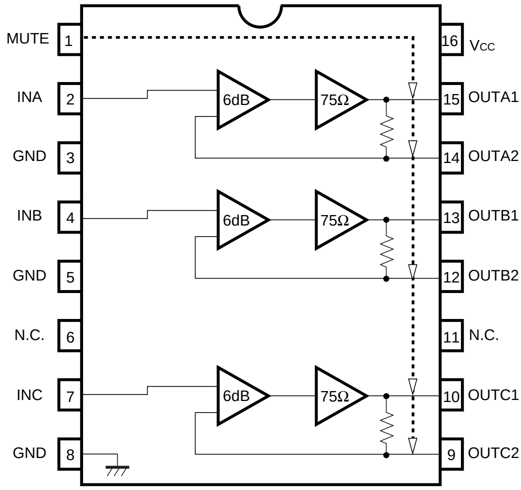
Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	8	V
Power dissipation	Pd	650	mW
Operating temperature	Topr	– 25 ~ + 75	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	Vcc	4.5	5.0	5.5	V

●Block diagram

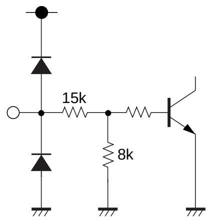
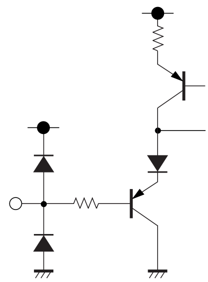
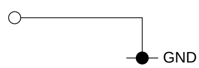
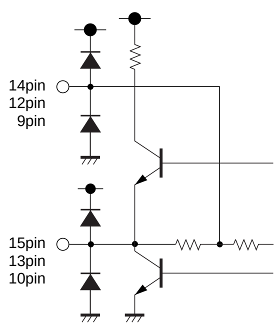
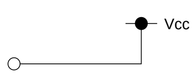
Multimedia ICs **BA7660FS**



MUTE (1pin)	
H	3ch MUTE
L	NORMAL

Multimedia ICs BA7660FS

●Pin descriptions and input / output circuits

Pin. No	Pin name	IN	OUT	Reference voltage	Equivalent circuit	Function
1	MUTE	○	—	—		Muting control If MUTE (pin 1) is set to HIGH, muting is carried out simultaneously on all three channels.
2 4 7	INA INB INC	○	—	—		Signal input Input signals consist of composite video signals, Y signals, C signals, RGB, and others. The input level is within a range of 0 to 1.3 (min.) to 1.5 (typ.).
3 5 8	GND	—	—	0V		Ground
14 12 9 15 13 10	OUTA2 OUTB2 OUTC2 OUTA1 OUTB1 OUTC1	—	○	0.9V 0.95V		Signal output The signal output level is (0.9 + 2 × input voltage [V]). Pins 9, 12, and 14 are the pins for sag correction. If pins 10, 13, and 15 are set to 0.2V or less, the protective circuit is triggered and the power-saving mode is accessed.
16	VCC	—	—	5.0V		Power supply

Features

- **Medium-voltage and Standard-voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
- **Automotive Temperature Range –40°C to 125°C**
- **Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **400 kHz (2.7V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes**
- **Partial Page Writes are Allowed**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP Packages**

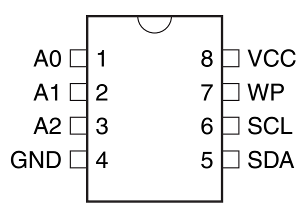
Description

The AT24C01A/02/04/08A/16A provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08A/16A is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP packages and is accessed via a two-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) versions.

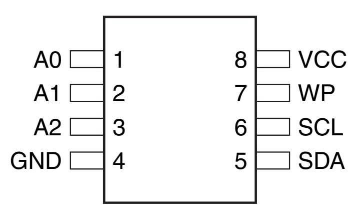
Table 1. Pin Configurations

Pin Name	Function
A0 – A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

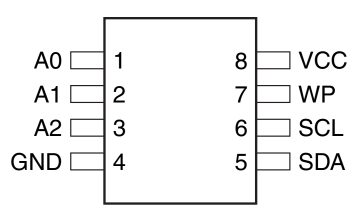
8-lead PDIP



8-lead SOIC



8-lead TSSOP



Two-wire Automotive Temperature Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08A
AT24C16A

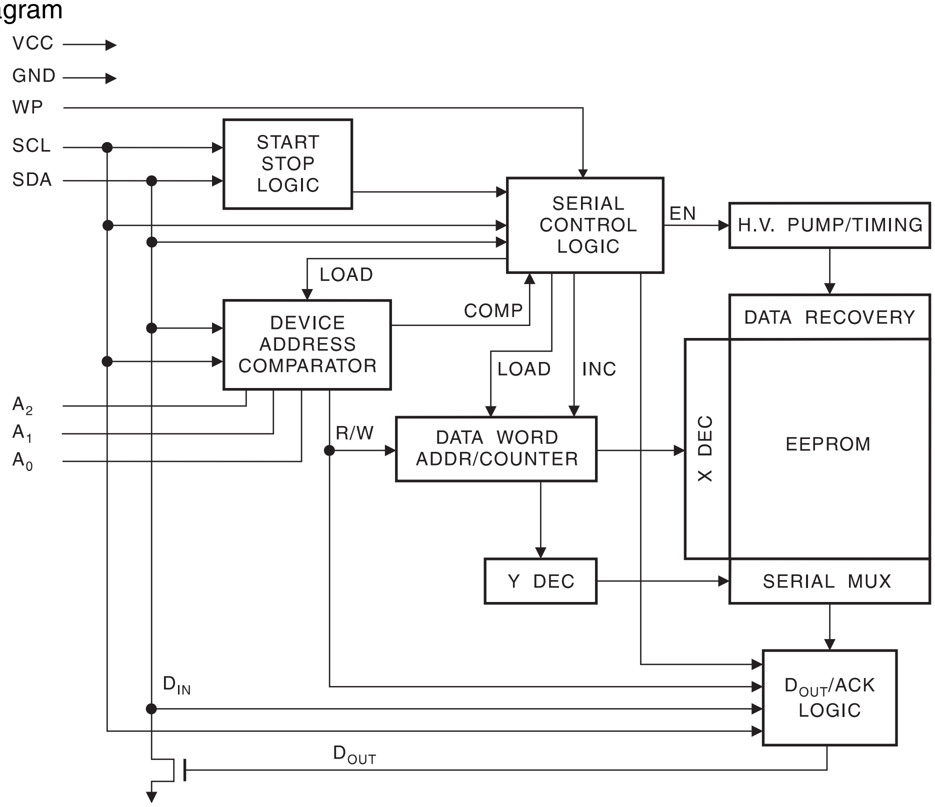
5092B–SEEPR–9/05

Absolute Maximum Ratings

Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

AT24C01A/02/04/08A/16A

The AT24C08A only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16A does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/08A/16A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

Table 2. Write Protect

WP Pin Status	Part of the Array Protected				
	24C01A	**24C02**	**24C04**	**24C08A**	**24C16A**
At V_{CC}	Full (1K) Array	Full (2K) Array	Full (4K) Array	Full (8K) Array	Full (16K) Array
At GND	Normal Read/Write Operations				

Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08A, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

AT24C16A, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

Device Addressing

The 1K, 2K, 4K, 8K and 16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see to Figure 7 on page 9).

The device address word consists of a mandatory “1”, “0” sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 1K/2K EEPROM. These 3 bits must compare to their corresponding hardwired input pins.

The 4K EEPROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hardwired input pins. The A0 pin is no connect.

The 8K EEPROM only uses the A2 device address bit with the next two bits being for memory page addressing. The A2 bit must compare to its corresponding hardwired input pin. The A1 and A0 pins are no connect.

The 16K does not use any device address bits but instead the three bits are used for memory page addressing. These page addressing bits on the 4K, 8K and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a “0”. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8 on page 10).

PAGE WRITE: The 1K/2K EEPROM is capable of an 8-byte page write, and the 4K, 8K and 16K devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (1K/2K) or fifteen (4K, 8K, 16K) more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 9 on page 10).

The data word address lower three (1K/2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (1K/2K) or sixteen (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves send-

ing a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a “0”, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 10 on page 10).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 11 on page 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 12 on page 11).

Figure 7. Device Address

1K/2K	1	0	1	0	A_2	A_1	A_0	R/W
	MSB							LSB
4K	1	0	1	0	A_2	A_1	P0	R/W
8K	1	0	1	0	A_2	P1	P0	R/W
16K	1	0	1	0	P2	P1	P0	R/W

Figure 8. Byte Write

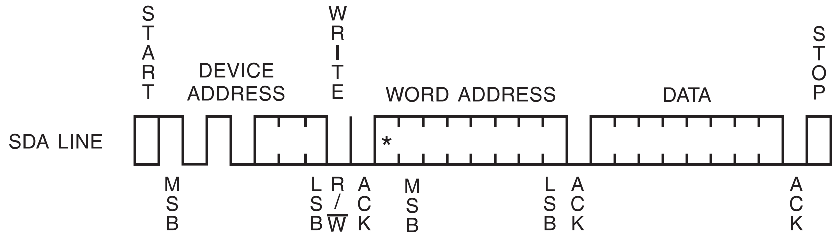
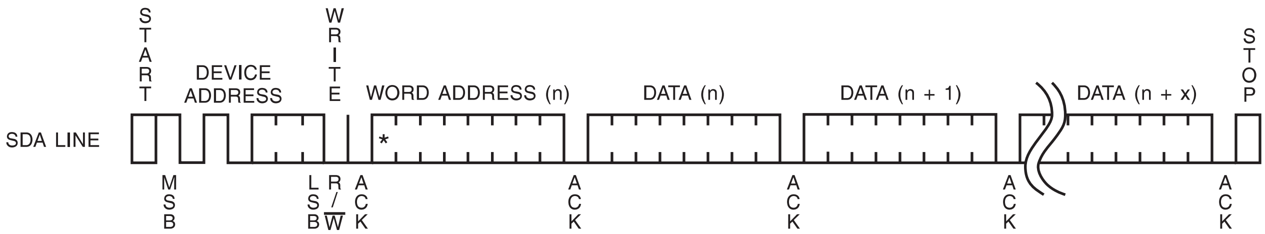


Figure 9. Page Write



(* = DON'T CARE bit for 1K)

Figure 10. Current Address Read

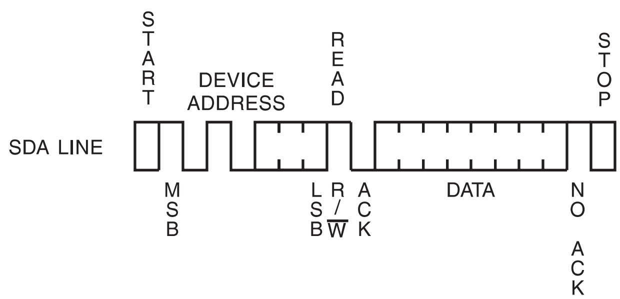
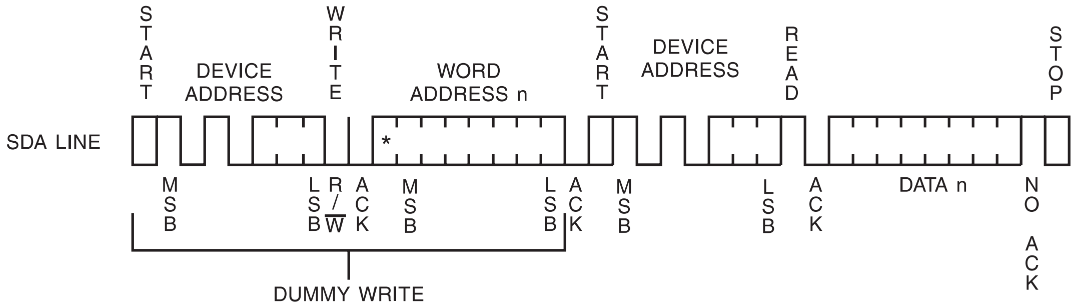
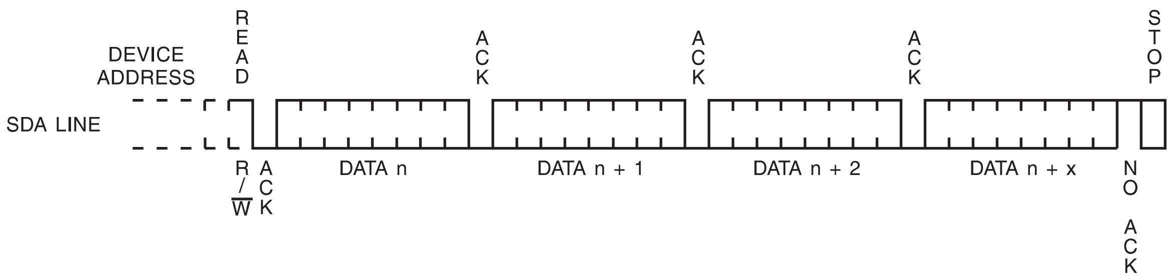


Figure 11. Random Read



(* = DON'T CARE bit for 1K)

Figure 12. Sequential Read



AM5888S
Motor Driver ICs

5-channel BTL Driver for DVD player AM5888S

The AM5888S is a five-channel BTL driver IC for driving the motors and actuators such as used in DVD player and consists of two independent precision voltage regulators with adjustable range from 1.5V to 4 V. It supports a variety of applications. Also, Pb free package is selectable (Please refer to Marking Identification).

- **Applications**

BTL driver for CD, CD-ROM and DVD.

- **Features**

1) Two channels are voltage-type BTL drivers for actuators of tracking and focus. Two channels are voltage-type BTL driver for sled and spindle motors. It is also built-in one channel bi-direction DC motor driver for tray.
2) Wide dynamic range [9.0V (*typ.*) when Vcc1= Vcc2= 12V, at R_L= 20Ω load].
3) Separating power of Vcc1 and Vcc2 is to improve power efficiency by a low supply voltage for tracking, focus, and spindle.
4) Level shift circuit built-in.
5) Thermal shut down circuit built-in.
6) Mute mode built-in.
7) **Dual actuator drivers:**
   A general purpose input OP provides differential input for signal addition. The output structure is two power OPAMPS in bridge configuration.
8) **Sled motor driver:**
   A general purpose input OP provides differential input for signal addition. The output structure is one power OPAMP in bridge configuration.
9) **Spindle driver:**
   Single input linear BTL driver. The output structure are two power OPAMPS in bridge configuration.
10) **Tray in-out driver:**
    The DC motor driver supports forward/reverse control for tray motor.
11) 2 **Built-in regulator controllers**
    Adjustable range 1.5V ~ 4V

AM5888S
Motor Driver ICs

Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc1 Vcc2	13.5	V
Power dissipation	P_d	*1.7	W
Operate Temp range	T_{opr}	-35 ~ +85	℃
Storage Temp range	T_{stg}	**-55 ~ +150	℃

*When mounted on a 70mm×70mm×1.6mm glass epoxy board.

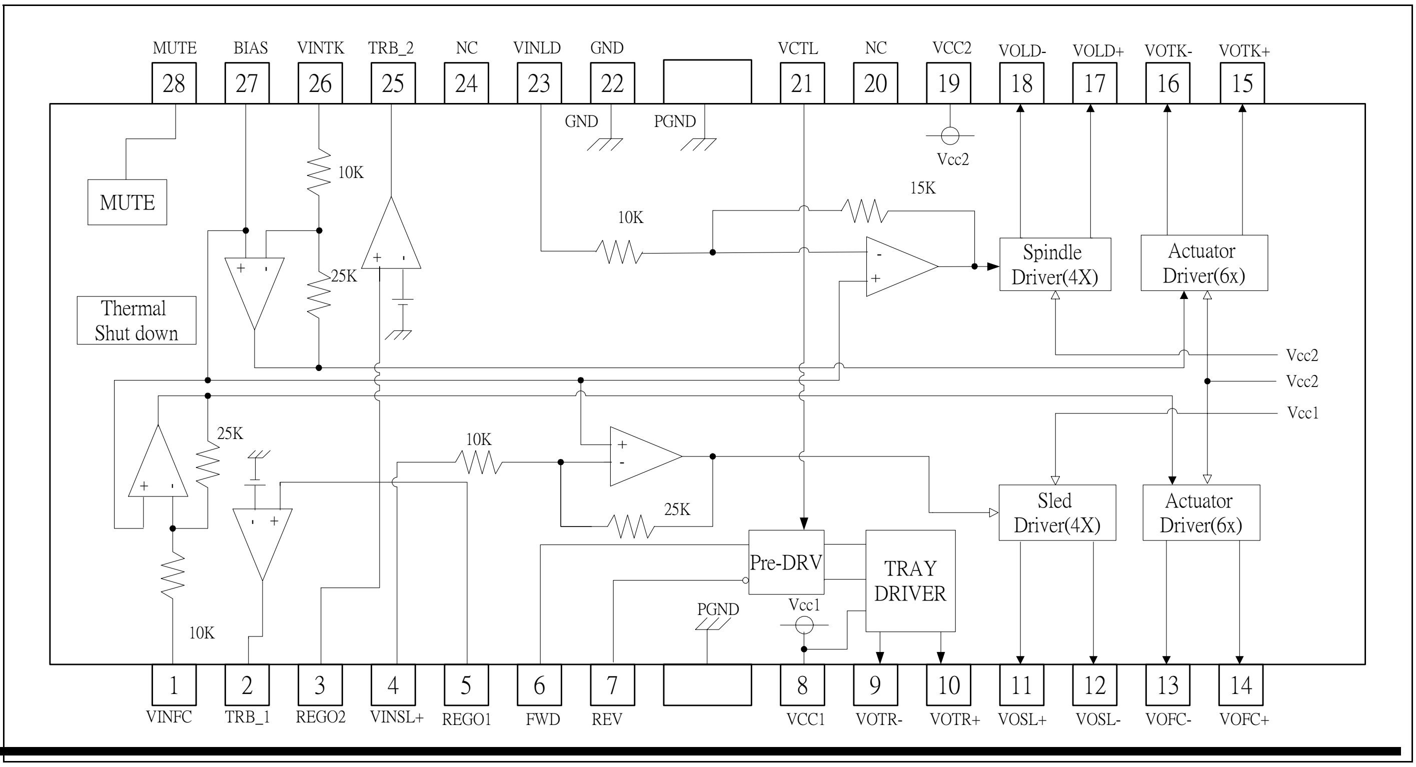
*Reduced by 13.6mW for each increase in T_a of 1℃ over 25℃.

**Should not exceed Pd or ASO and T_j=150°C values

Guaranteed operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc1	4.3 ~ 13.2	V
	Vcc2	4.3 ~ Vcc1	V

Block diagram



AM5888S
Motor Driver ICs

Pin description

PIN No	Pin Name	Function
1	VINFC	Input for focus driver
2	TRB_1	Connect to external transistor base
3	REGO2	Regulator voltage output, connect to external transistor collector
4	VINSL+	Input for the sled driver
5	REGO1	Regulator voltage output, connect to external transistor collector
6	FWD	Tray driver forward input
7	REV	Tray driver reverse input
8	Vcc1	Vcc for pre-drive block and power block of sled and tray
9	VOTR-	Tray driver output (-)
10	VOTR+	Tray driver output (+)
11	VOSL+	Sled driver output (+)
12	VOSL-	Sled driver output (-)
13	VOFC-	Focus driver output (-)
14	VOFC+	Focus driver output (+)
15	VOTK+	Tracking driver output (+)
16	VOTK-	Tracking driver output (-)
17	VOLD+	Spindle driver output (+)
18	VOLD-	Spindle driver output (-)
19	Vcc2	Vcc for power block of spindle, tracking and focus
20	NC	No Connection
21	VCTL	Speed control input of tray driver
22	GND	Ground
23	VINLD	Input for spindle driver
24	NC	No Connection
25	TRB_2	Connect to external transistor base
26	VINTK	Input for tracking driver
27	BIAS	Input for reference voltage
28	MUTE	Input for mute control

Notes) Symbol of + and – (output of drivers) means polarity to input pin.
(For example, if voltage of pin1 is high, pin14 is high.)

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

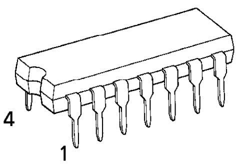
TC74HCT7007AP, TC74HCT7007AF

HEX BUFFER

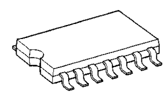
The TC74HCT7007A is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
The internal circuit is composed of 4 stages including a buffer output, which provides high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed ········ t_{pd} = 11ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ········ I_{CC} = 1μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ···· V_{IH} = 2V (Min.)
  V_{IL} = 0.8V (Max.)
- Wide Interfacing ability ········ LSTTL, NMOS, CMOS
- Output Drive Capability ········ 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$ = I_{OL} = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS07

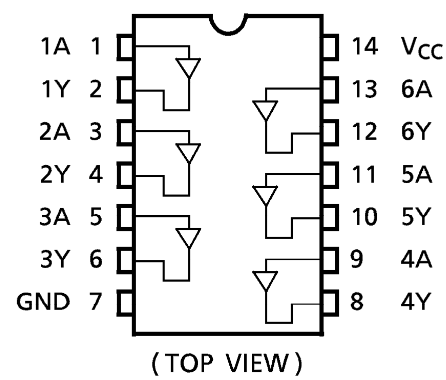


14
1
P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)

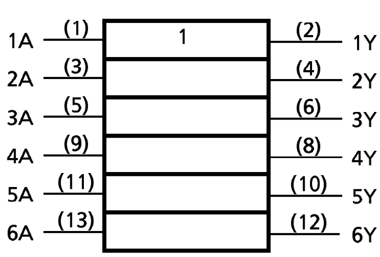


14
1
F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



PIN ASSIGNMENT

A	Y
L	L
H	H

961001EBA2

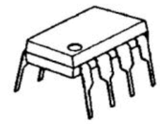
NJM2068

LOW-NOISE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2068 is a high performance, low noise dual operational amplifier. This amplifier features popular pin-out, superior noise performance, and superior total harmonic distortion. This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product and slew rate, which far exceeds that of the 4558 type amplifier. The specially designed low noise input transistors allow the NJM2068 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifier.

■ PACKAGE OUTLINE



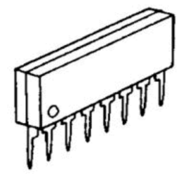
NJM2068D



NJM2068M



NJM2068V

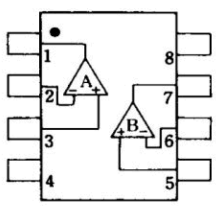


NJM2068L

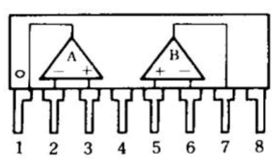
■ FEATURES

- Operating Voltage (±4V~±18V)
- Low Total Harmonic Distortion (0.001% typ.)
- Low Noise Voltage (FLAT+JISA,0.56µV typ.)
- High Slew Rate (6V/µs typ.)
- Unity Gain Bandwidth (27MHz @ f=10kHz)
- Package Outline DIP8,DMP8,SIP8,SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



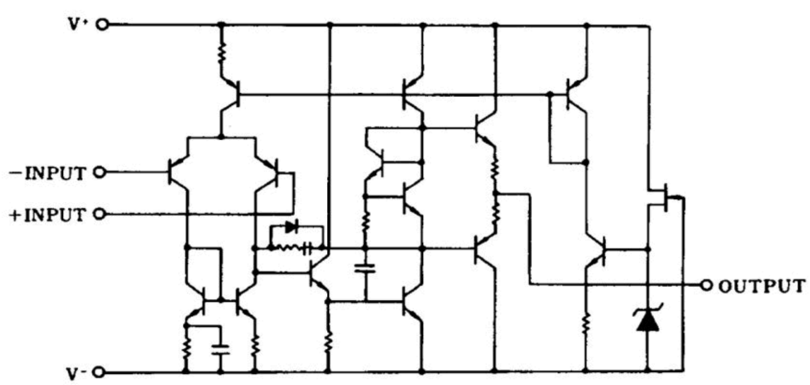
NJM2068D
NJM2068M
NJM2068V



NJM2068L

PIN FUNCTION
1.A OUTPUT
2.A –INPUT
3.A +INPUT
4.V^-
5.B +INPUT
6.B –INPUT
7.B OUTPUT
8.V^+

■ EQUIVALENT CIRCUIT (1/2 Shown)

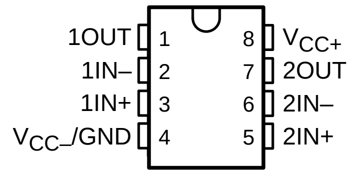


TL3472
HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/μs**
- **Fast Settling Time . . . 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground (V_{CC-})**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**

D OR P PACKAGE
(TOP VIEW)



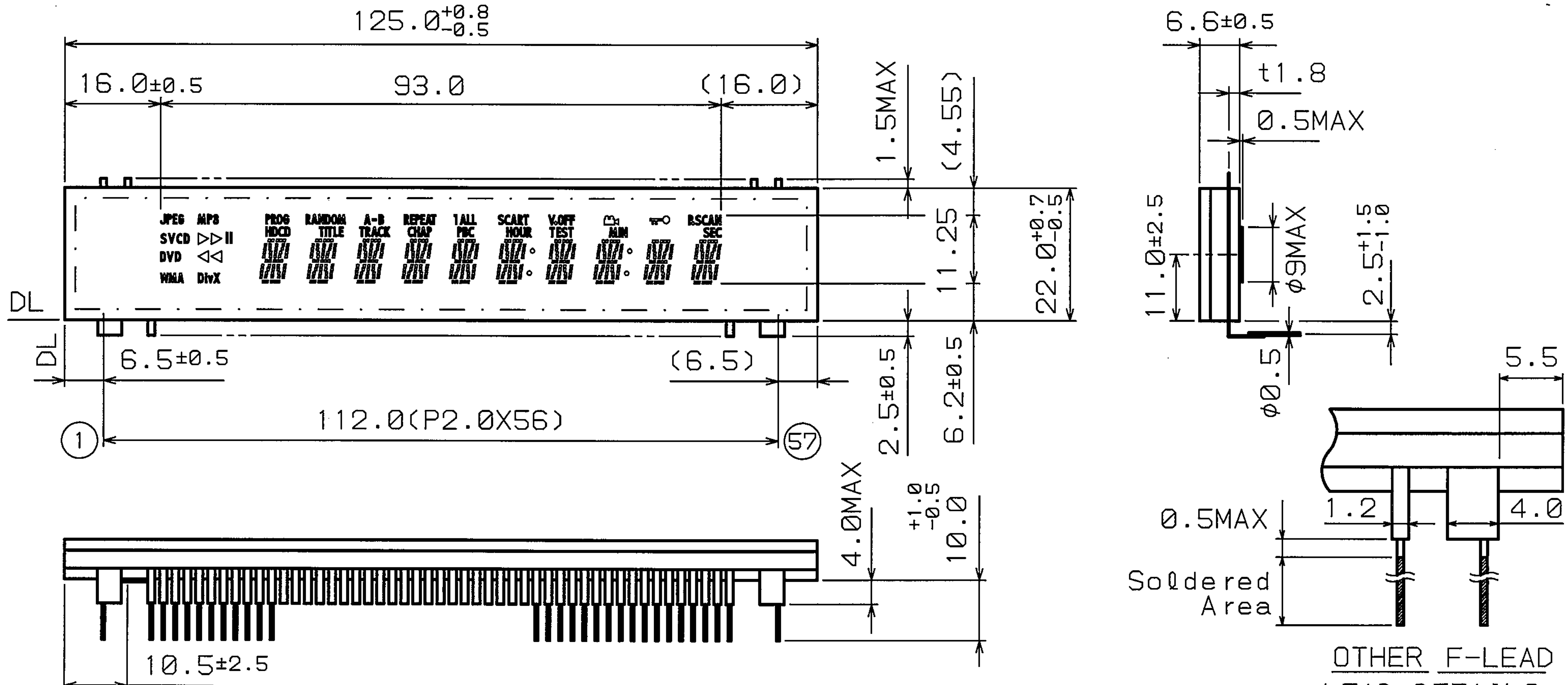
description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 25	TL3472CP	TL3472CP
	SOIC (D)	Tube of 50	TL3472CD	3472C
		Reel of 2500	TL3472CDR	
–40°C to 105°C	PDIP (P)	Tube of 25	TL3472IP	TL3472IP
	SOIC (D)	Tube of 50	TL3472ID	Z3472
		Reel of 2500	TL3472IDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



LEAD FREE SOLDER

PIN CONNECTION

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
CONNECTION	F-	NX	NP	NP	1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	NX	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4

PIN NO.	51	52	53	54	55	56	57
CONNECTION	P3	P2	P1	NP	NP	NX	F+

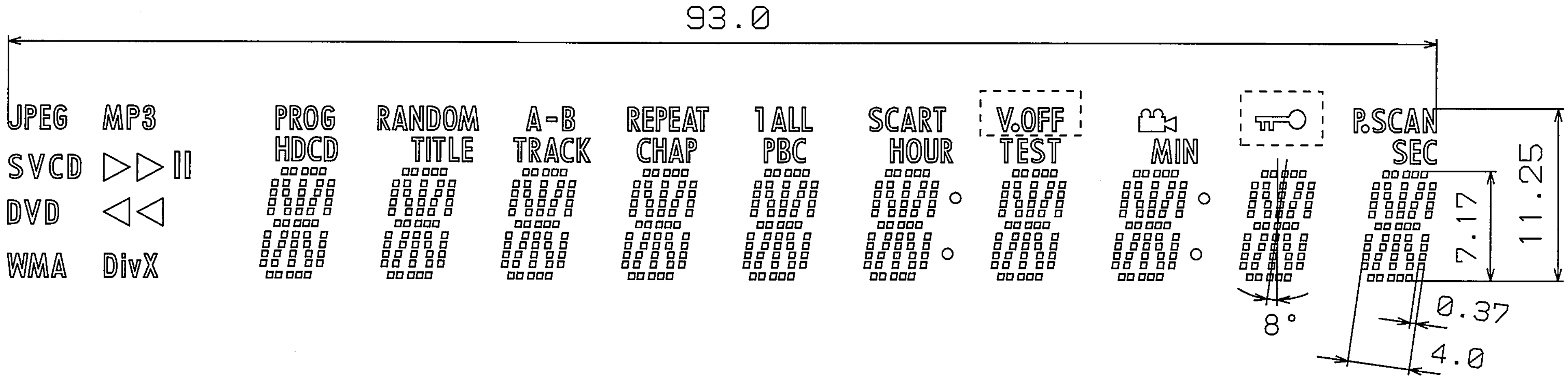
NOTE
1) F−,F+ --- Filament
2) NP ------- No pin
3) NX ------- No extend pin
4) DL ------- Datum Line
5) 1G~xG --- Grid
6) Solder composition is Sn-3Ag-0.5Cu.
7) Field of vision is a minimum of 9.5° from the upper side.

(unit in mm)

11-BT-242GNK
OUTER DIMENSION

-4-

PATTERN DETAIL



COLOR OF ILLUMINATION

Red (R. x=0.67,y=0.33) ------- Within dotted lines.

Green (G. x=0.24,y=0.41) ------ All other graphics.

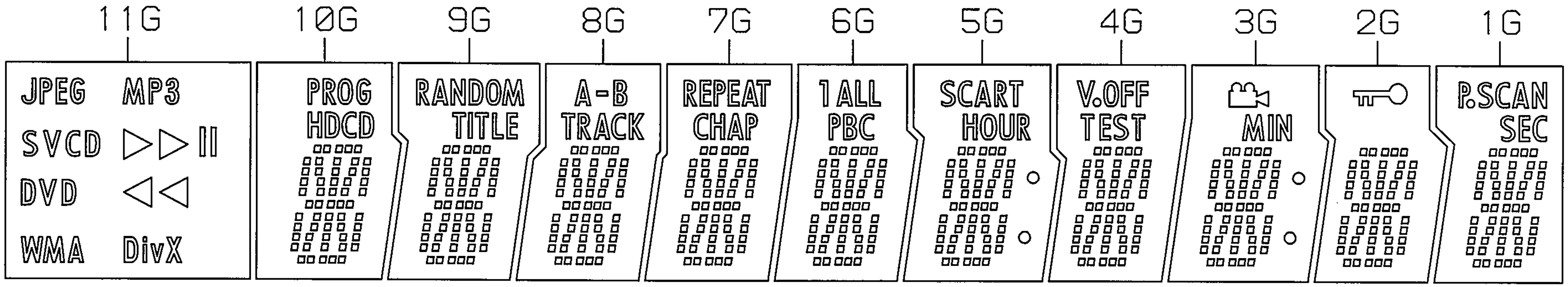
The expected life time of Red phosphor is 30,000Hours.
(The definition of the life end is minimum value specified of the luminance)
Cadmium Free Phosphor used.

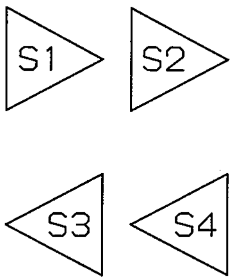
(unit in mm)

11-BT-242GNK
PATTERN DETAIL
COLOR OF ILLUMINATION

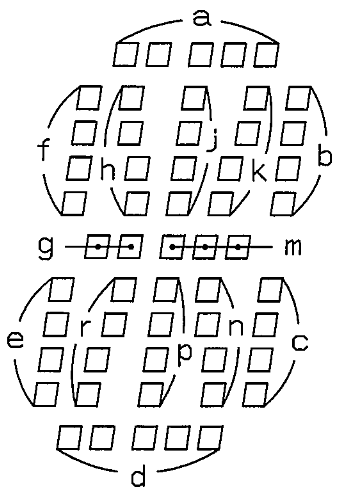
-5-

GRID ASSIGNMENT





(11G)



(10G~1G)



(5G,3G)

11-BT-242GNK
GRID ASSIGNMENT

-9-

ANODE_CONNECTION

	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G
P1	JPEG	PROG	RANDOM	A	REPEAT	1	SCART	V.OFF			P.SCAN
P2	MP3	HDCD	TITLE	-B	CHAP	ALL	HOUR	TEST	MIN	-	SEC
P3	S	-	-	TRACK	-	PBC	col	-	col	-	-
P4	V	a	a	a	a	a	a	a	a	a	a
P5	CD	f	f	f	f	f	f	f	f	f	f
P6	II	h	h	h	h	h	h	h	h	h	h
P7	DVD	j	j	j	j	j	j	j	j	j	j
P8	WMA	k	k	k	k	k	k	k	k	k	k
P9	DivX	b	b	b	b	b	b	b	b	b	b
P10	S1	m	m	m	m	m	m	m	m	m	m
P11	S2	g	g	g	g	g	g	g	g	g	g
P12	S3	n	n	n	n	n	n	n	n	n	n
P13	S4	p	p	p	p	p	p	p	p	p	p
P14	-	r	r	r	r	r	r	r	r	r	r
P15	-	c	c	c	c	c	c	c	c	c	c
P16	-	e	e	e	e	e	e	e	e	e	e
P17	-	d	d	d	d	d	d	d	d	d	d

-7-

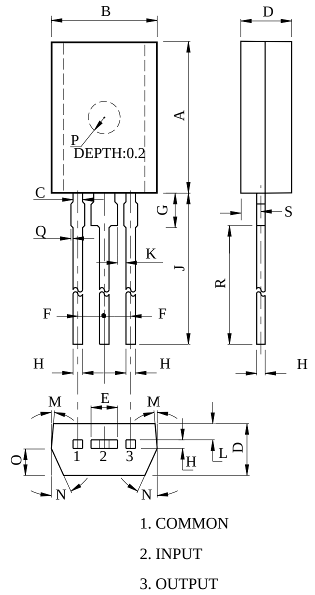
11-BT-242GNK
ANODE CONNECTION

KEC

SEMICONDUCTOR
TECHNICAL DATA

KIA79L05BP~ KIA79L24BP
BIPOLAR LINEAR INTEGRATED CIRCUIT

THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V.



DIM	MILLIMETERS
A	7.20 MAX
B	5.20 MAX
C	0.60 MAX
D	2.50 MAX
E	1.15 MAX
F	1.27
G	1.70 MAX
H	0.55 MAX
J	14.00±0.50
K	0.35 MIN
L	0.75±0.10
M	4°
N	25°
O	1.25
P	Φ1.50
Q	0.10 MAX
R	12.50±0.50
S	1.00

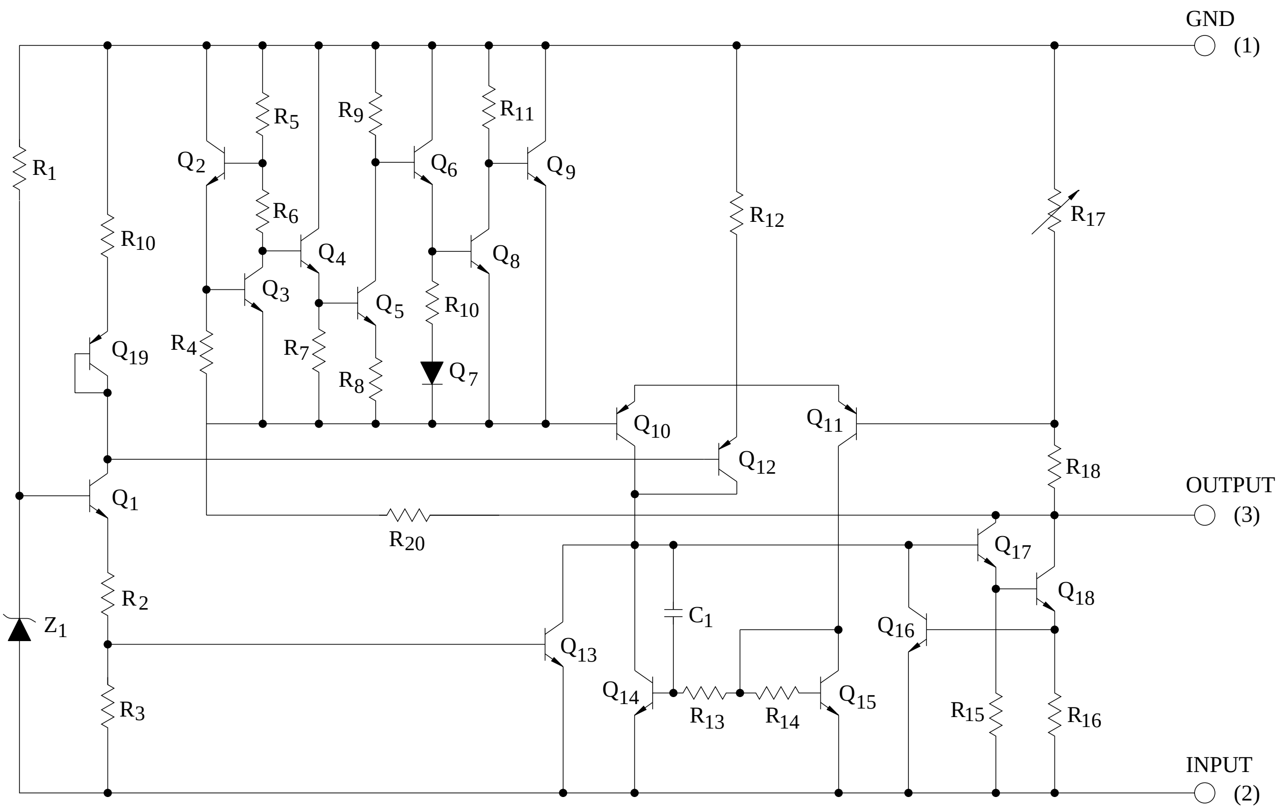
TO-92L

FEATURES
· Best Suited to a Power Supply for TTL and CMOS.
· Built-in Overcurrent Protective Circuit.
· Built-in Thermal Protective Circuit.
· Max. Output Current 150mA (T_j=25 ℃).
· Packaged in TO-92L.

MAXIMUM RATINGS (Ta=25 ℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	KIA79L05BP ~ KIA79L15BP	V_{IN}	-35	V
	KIA79L18BP ~ KIA79L24BP		-40	
Power Dissipation (Tc=25 ℃)		P_D	800	mW
Operating Junction Temperature		T_j	-30 ~ 150	℃
Operating Temperature		T_{opr}	-30 ~75	℃
Storage temperature		T_{stg}	-55 ~ 150	℃

EQUIVALENT CIRCUIT



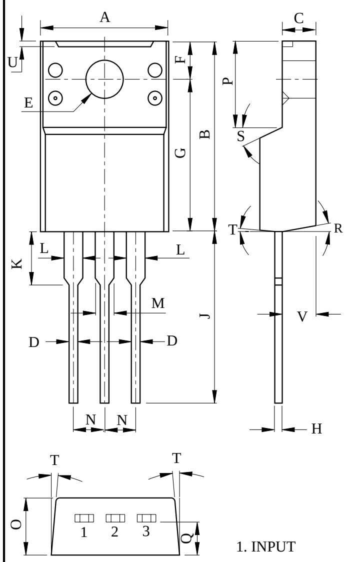
KEC

SEMICONDUCTOR
TECHNICAL DATA

KIA7805API~ KIA7824API

BIPOLAR LINEAR INTEGRATED CIRCUIT

THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V.



DIM	MILLIMETERS
A	10.30 MAX
B	15.30 MAX
C	2.70±0.30
D	0.85 MAX
E	Φ3.20±0.20
F	3.00±0.30
G	12.30 MAX
H	0.75 MAX
J	13.60±0.50
K	3.90 MAX
L	1.20
M	1.30
N	2.54
O	4.50±0.20
P	6.80
Q	2.60±0.20
R	10°
S	25°
T	5°
U	0.5
V	2.60±0.15

1. INPUT
2. COMMON
3. OUTPUT

TO-220IS

FEATURES

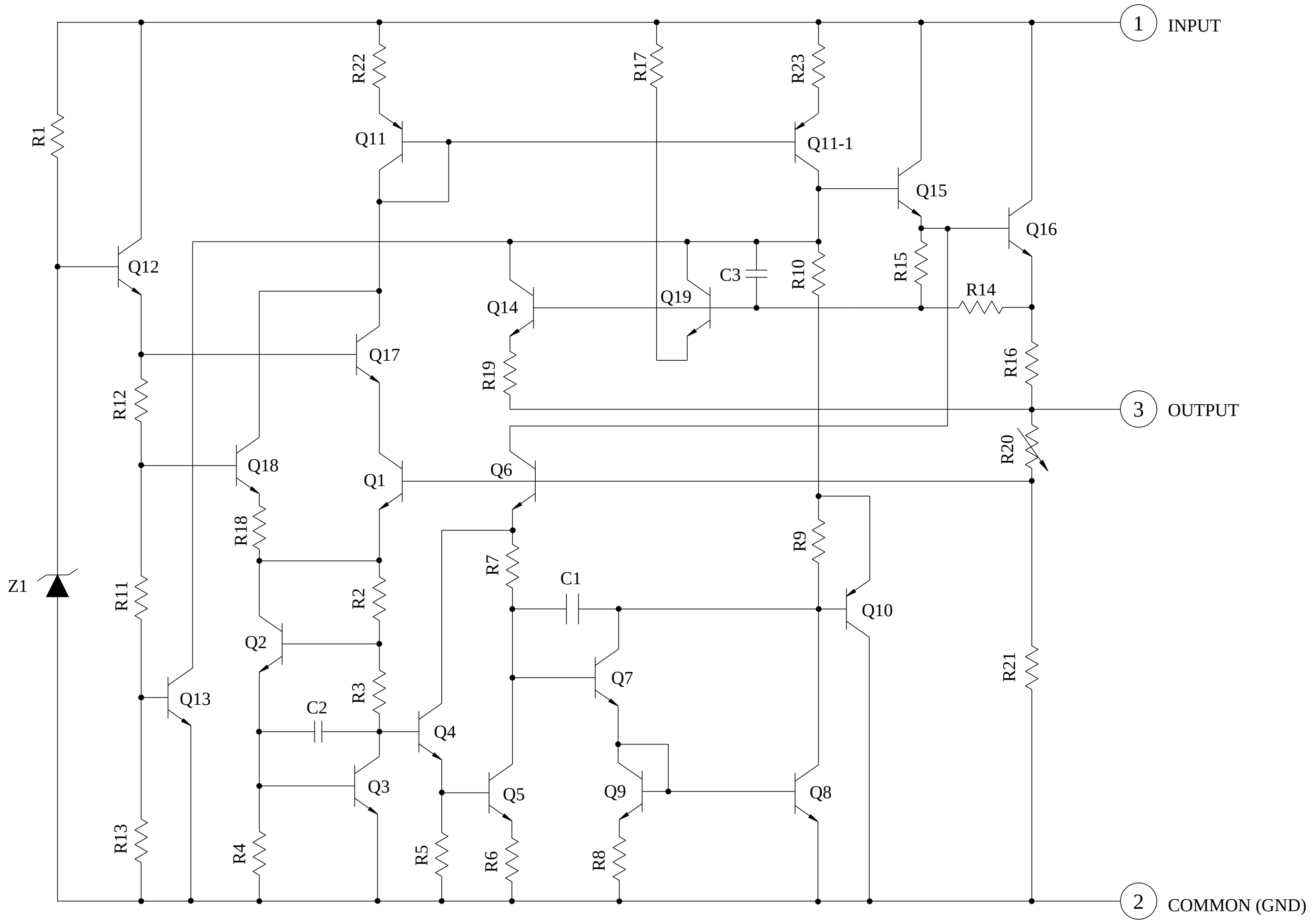
- Suitable for C-MOS, TTL, the Other Digital IC's Power Supply.
- Internal Thermal Overload Protection.
- Internal Short Circuit Current Limiting.
- Output Current in Excess of 1A.
- Satisfies IEC-65 Specification. (International Electronical Commission)

MAXIMUM RATINGS (Ta=25 ℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	KIA7805API ~ KIA7815API	V_{IN}	35	V
	KIA7818API ~ KIA7824API		40	
Power Dissipation (Tc=25 ℃)		P_D	20.8	W
Power Dissipation (Without Heatsink)	KIA7805API ~ KIA7824API	P_D	2.0	W
Operating Junction Temperature		T_j	-30 ~150	℃
Storage Temperature		T_{stg}	-55 ~150	℃

KIA7805API~KIA7824API

EQUIVALENT CIRCUIT



Optic receiver modules

KODENSHI

KSM - 60 钡 TH2 · KSM - 70 钡 TH2

The KSM - 60钡TH2 consist of a PIN Photodiode of high speed and a preamplifier IC in the package as an receiver for Infrared remote control systems

FEATURES

- One mold small package
- 5 Volt supply voltage, low power consumption
- Shielded against electrical field disturbance
- High immunity against ambient light
- Easy interface with the main board
- TTL and CMOS compatibility

APPLICATIONS

- TV, VTR, Acoustic Devices, Air Conditioners, Car Stereo Units, Computers, Interior controlling appliances, and all appliances that require remote controlling

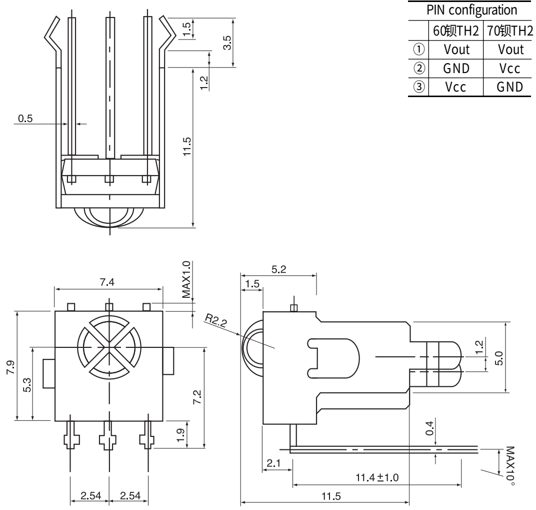
DIMENSIONS

(Unit : mm)

NOTE

PIN configuration

	60钡TH2	70钡TH2
①	Vout	Vout
②	GND	Vcc
③	Vcc	GND



MAXIMUM RATINGS

(Ta=25℃ Unless otherwise noted)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	5.5	V
Operating Temperature	Topr.	- 10~ +60	℃
Storage Temperature	Tstg.	- 20~ +75	℃
Soldering Temperature	Tsol.	260(Max 5 sec)	℃

B.P.F CENTER FREQUENCY

Model NO.	B.P.F Center Frequency(kHz)
KSM -◯◯1 TH2	40.0
KSM -◯◯2 TH2	36.7
KSM -◯◯3 TH2	37.9
KSM -◯◯4 TH2	32.7
KSM -◯◯5 TH2	56.9

ELECTRO-OPTICAL CHARACTERISTICS

(Ta=25℃), Vcc=5.0V

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit.
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
Current Consumption	I_{CC}	Input Signal=0		-	1.2	2.5	mA
Peak Wavelength *1	λp			-	940	-	nm
B.P.F Center Frequency	fo			-	37.9	-	kHz
Transmission Distance *1	L	200±50lx	0°	10	-	-	m
			±30°	7	-	-	m
H Level Output Voltage *1	V_{OH}	30cm over the ray axis		4.5	5.0	-	V
L Level Output Voltage *1	V_{OL}			-	0.1	0.5	V
H Level Output Pulse Width *1	T_{WH}	Burst Wave=600µs Period=1.2ms		500	600	700	µs
L Level Output Pulse Width *1	T_{WL}			500	600	700	µs
Output Form				Active Low Output			

Note : *1. It specifies the maximum distance between emitter and detector that the output waveform satisfies the standard under the conditions below against the standard transmitter

1) Measuring place : Indoor without extreme reflection of light
2) Ambient light source : Detecting surface illumination shall be irradiate 200±50lx under ordinary white fluorescence lamp without high frequency lightning
3) Standard transmitter : Burst wave of standard transmitter shall be arranged to 50mVp - p under the measuring circuit

National Semiconductor

October 2002

LM1117/LM1117I
800mA Low-Dropout Linear Regulator

General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in LLP, TO-263, SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

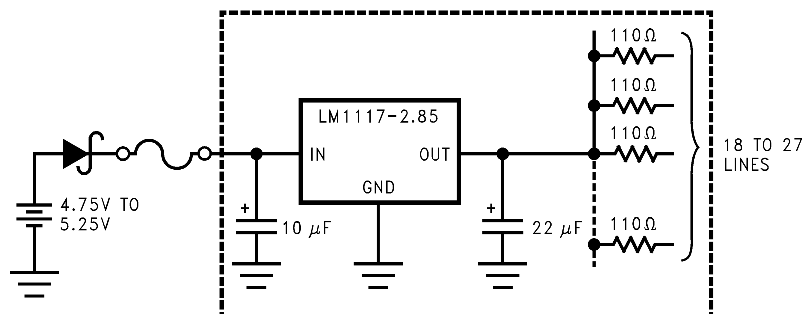
- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 and LLP Packages
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
  - — LM1117 0˚C to 125˚C
  - — LM1117I −40˚C to 125˚C

Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

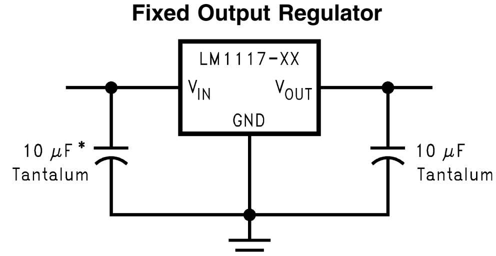
Typical Application

Active Terminator for SCSI-2 Bus



10091905

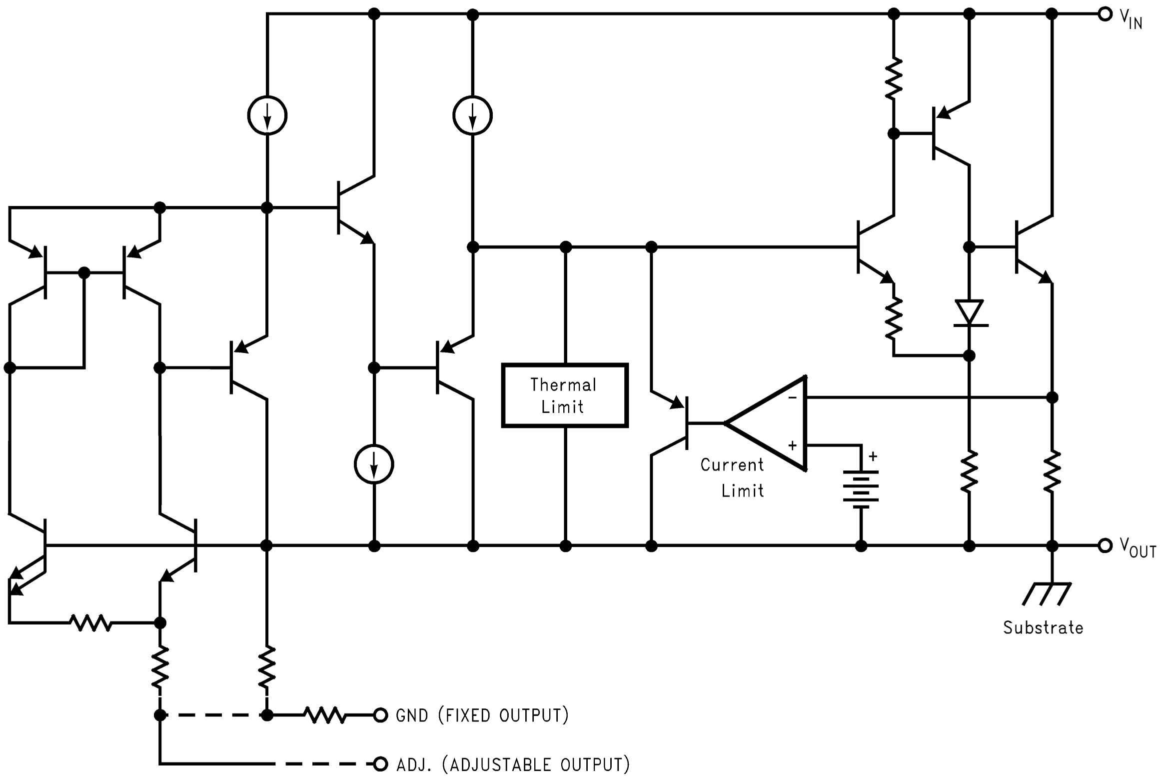
Fixed Output Regulator



* Required if the regulator is located far from the power supply filter.

10091928

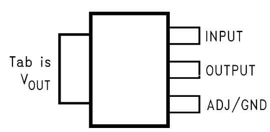
Block Diagram



10091901

Connection Diagrams

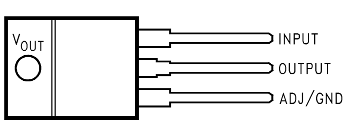
SOT-223



10091904

Top View

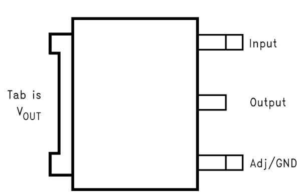
TO-220



10091902

Top View

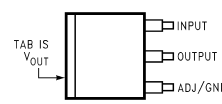
TO-252



10091938

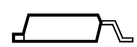
Top View

TO-263



10091944

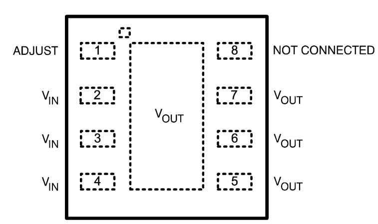
Top View



10091945

Side View

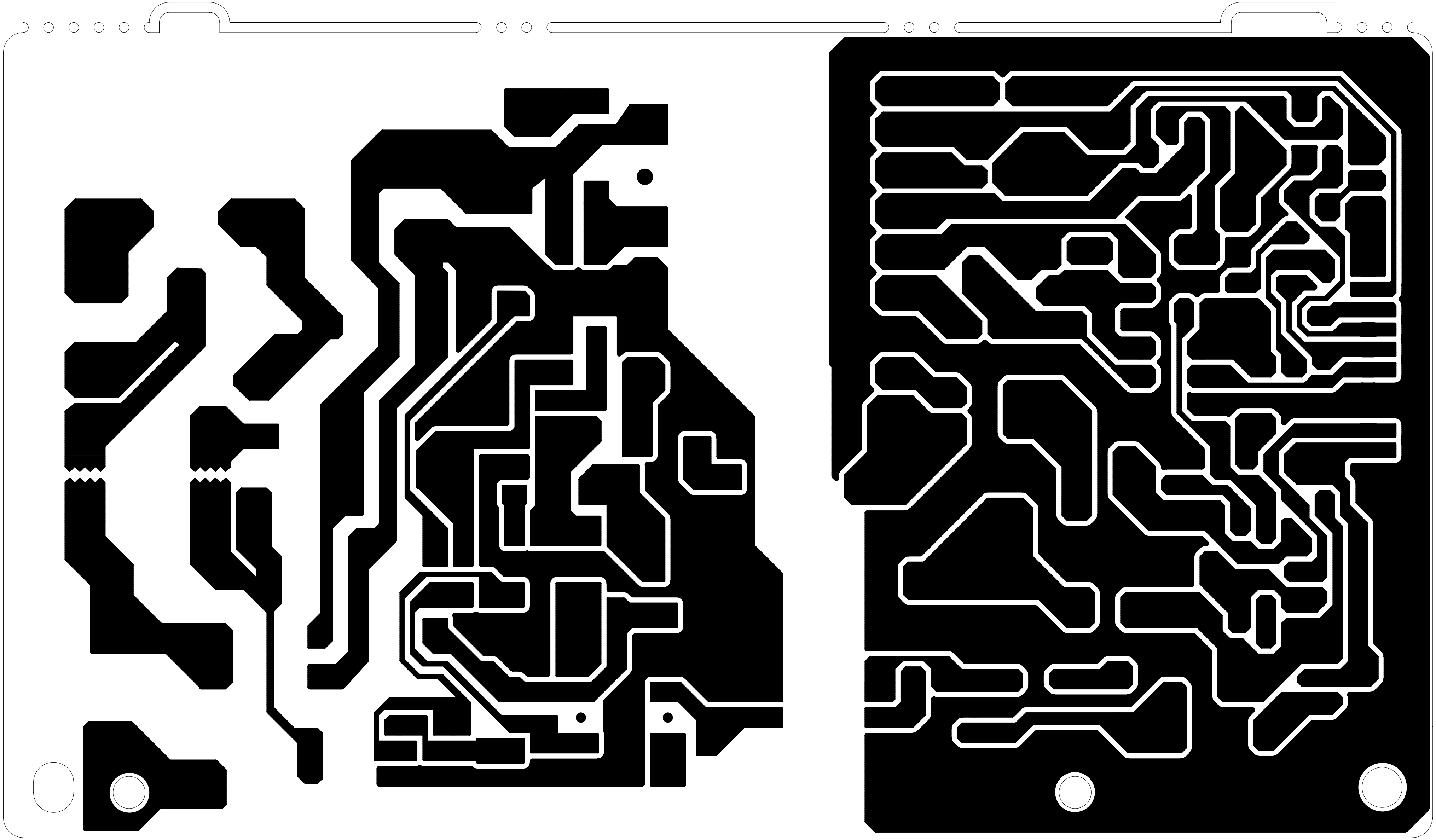
LLP



10091946

When using the LLP package
Pins 2, 3 & 4 must be connected together and
Pins 5, 6 & 7 must be connected together

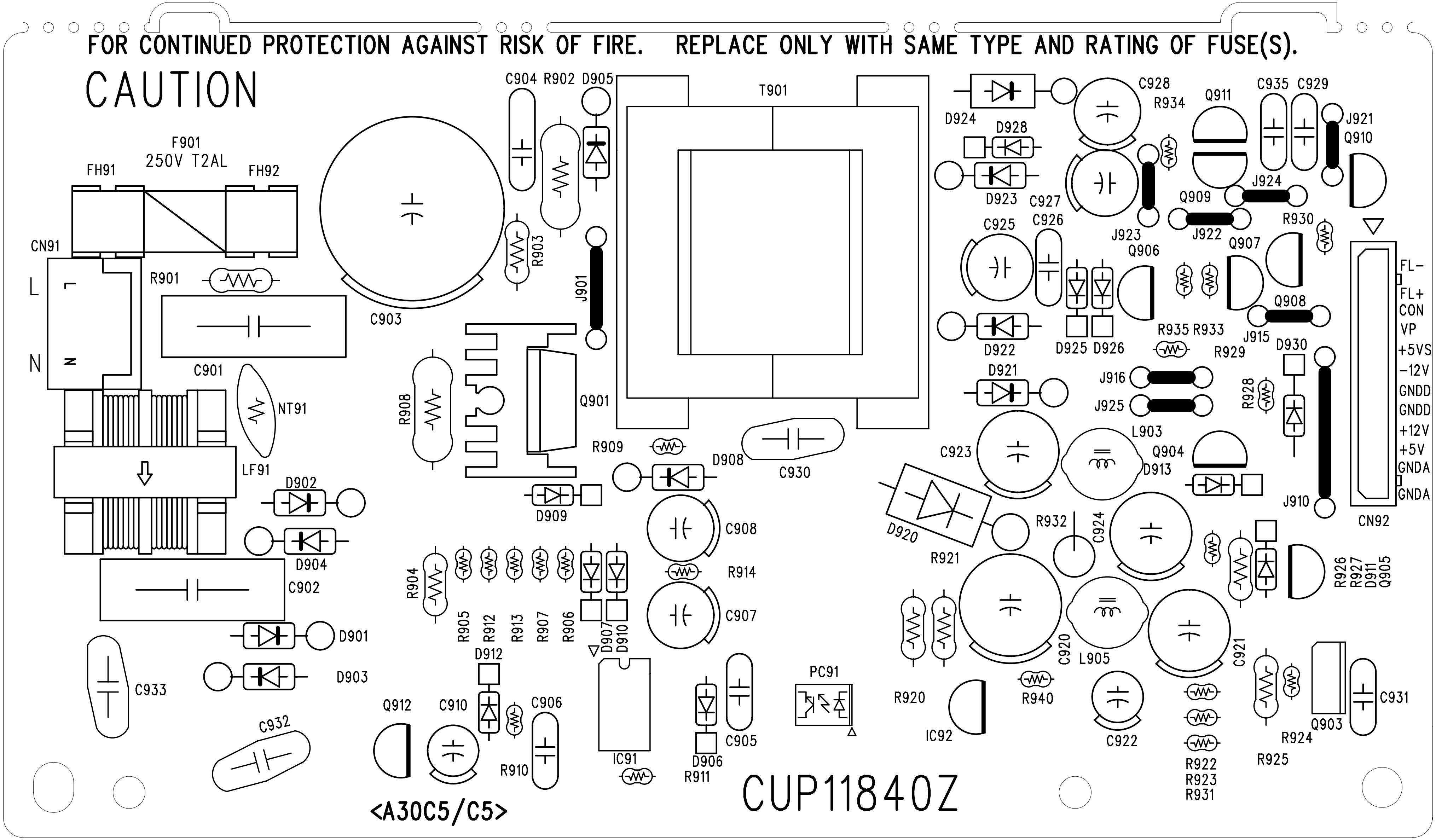
Top View



DVD 27-50629.pcb - Mon Dec 26 16:44:38 2005

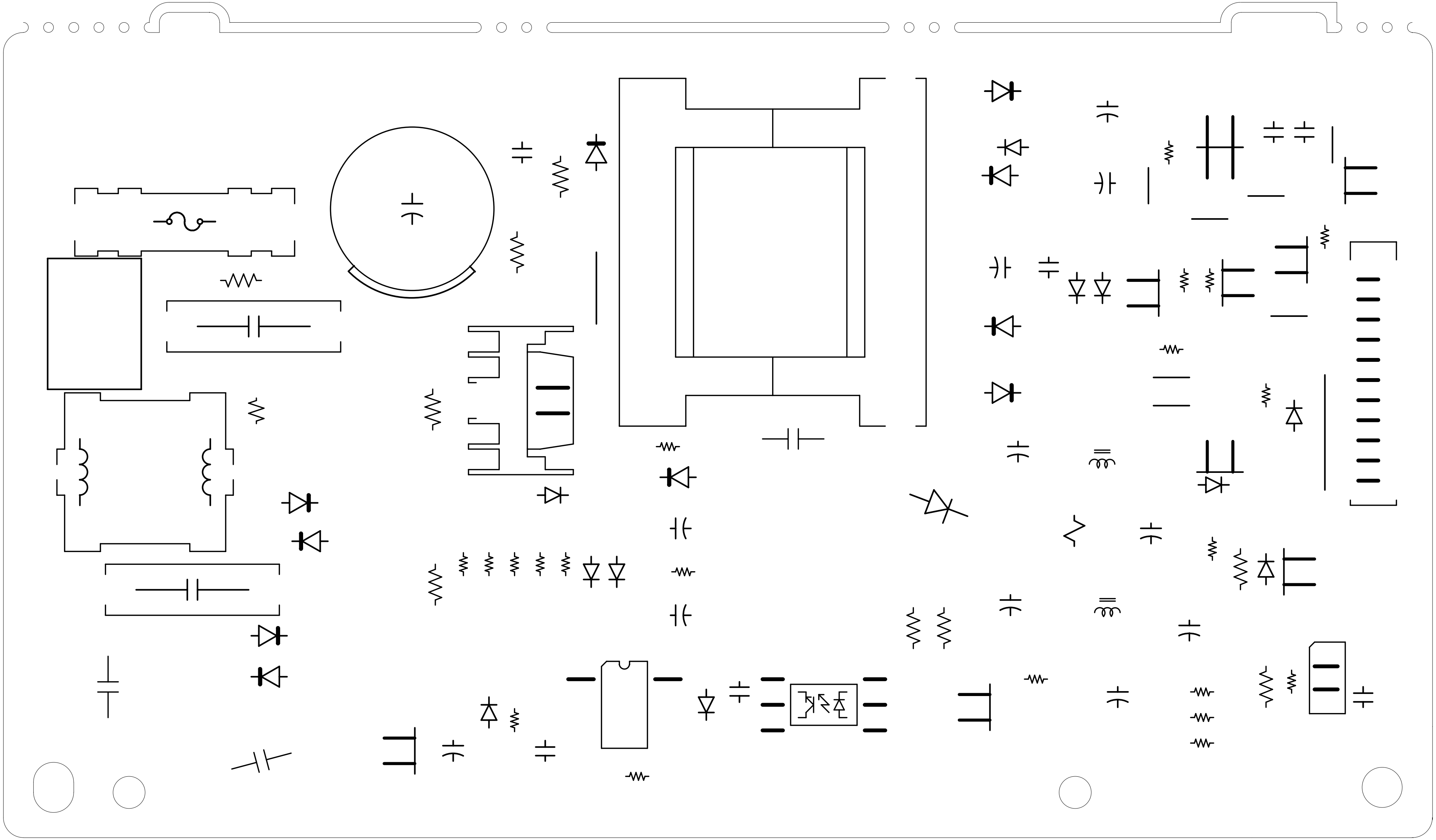
FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE AND RATING OF FUSE(S).

CAUTION

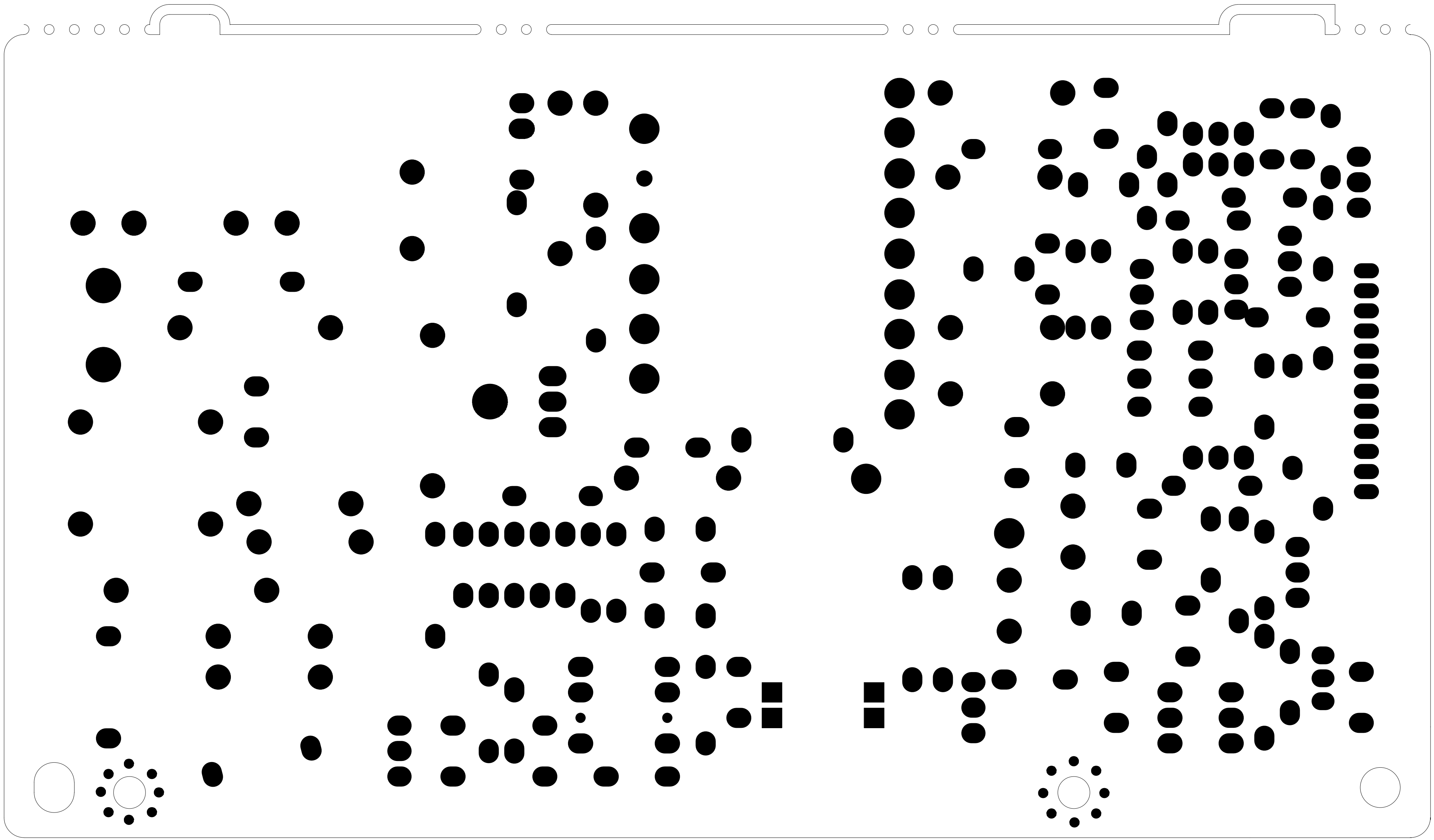


CUP11840Z

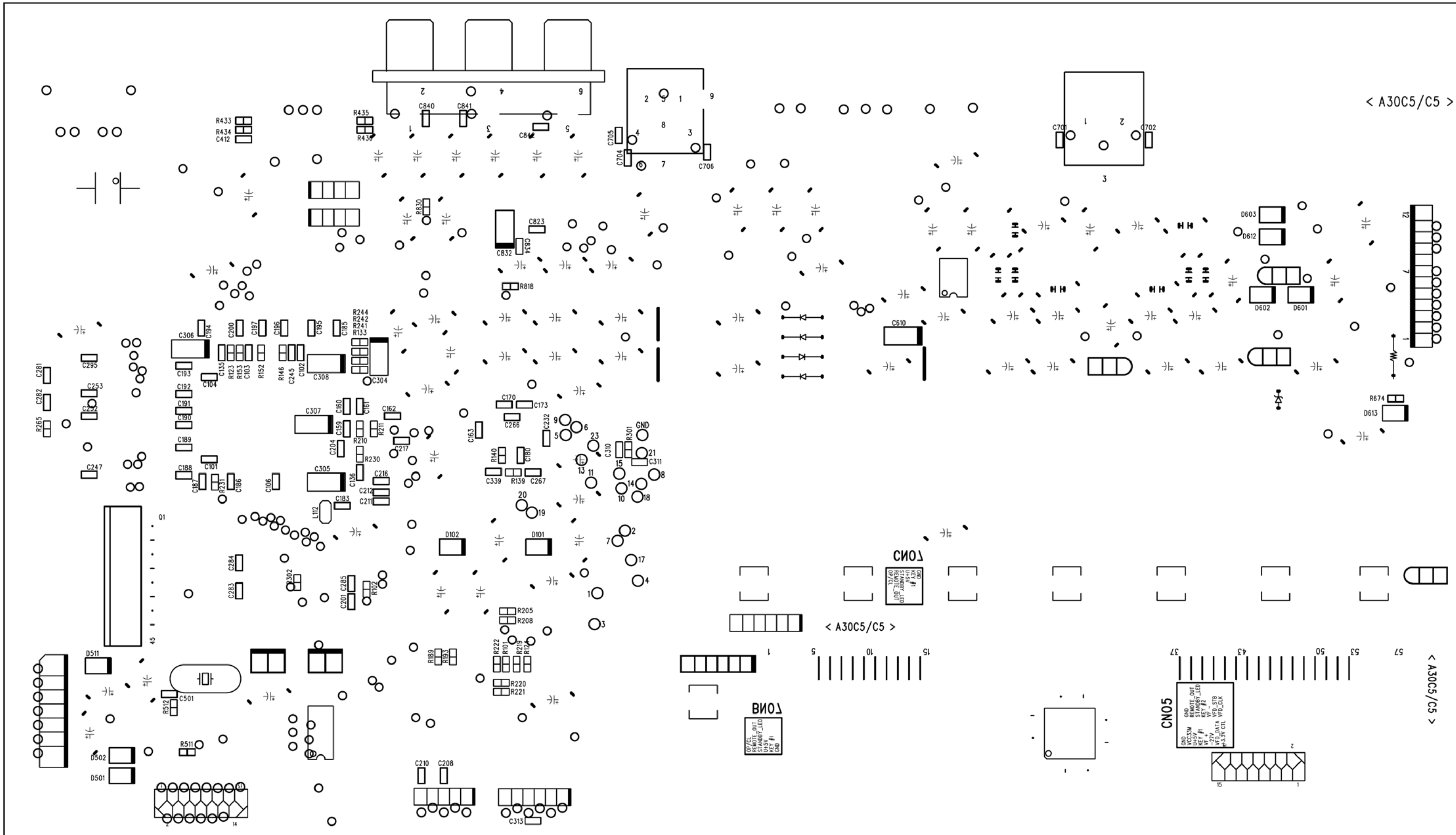
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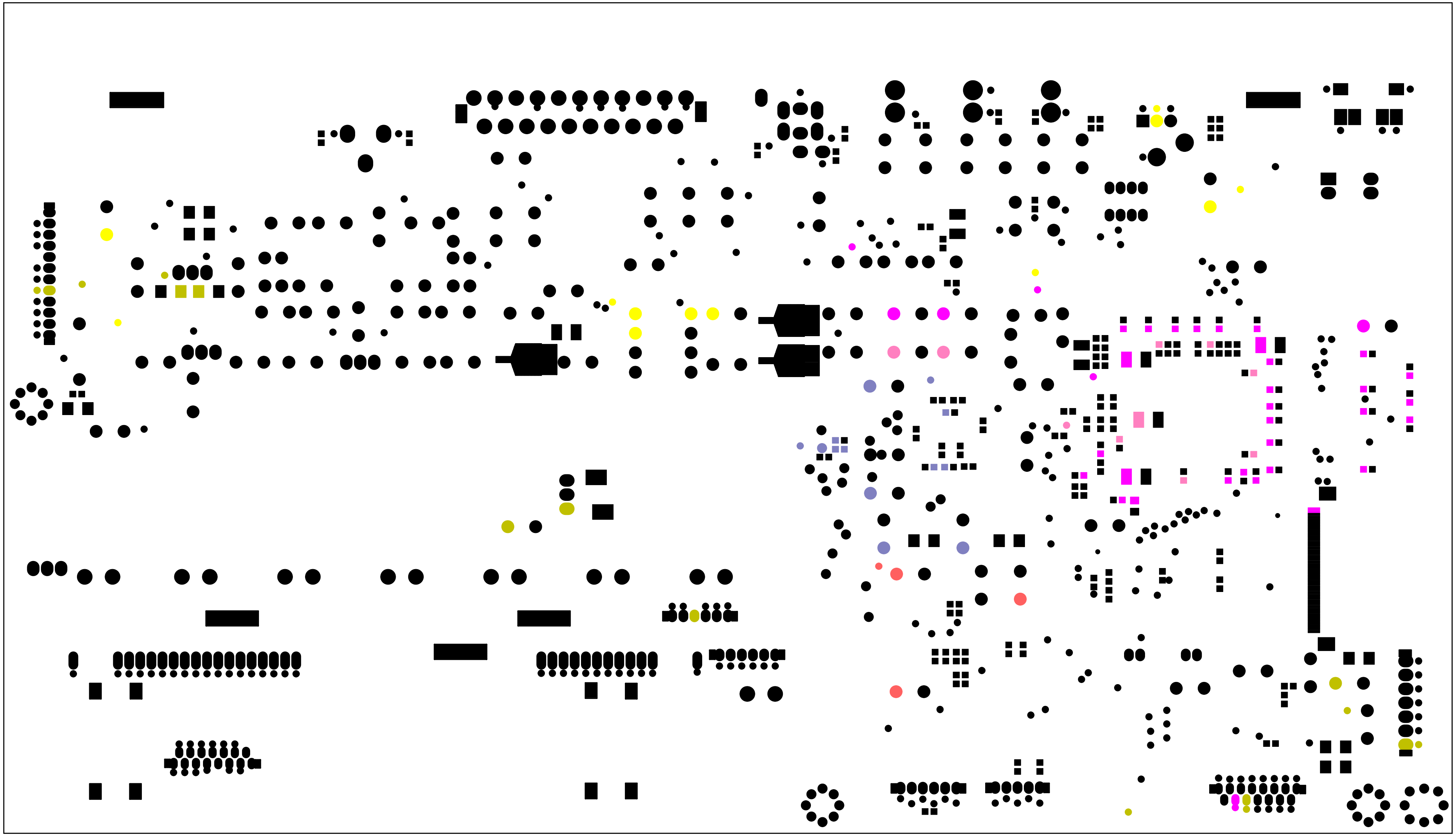


DVD 27-50629.pcb - Mon Dec 26 16:48:16 2005

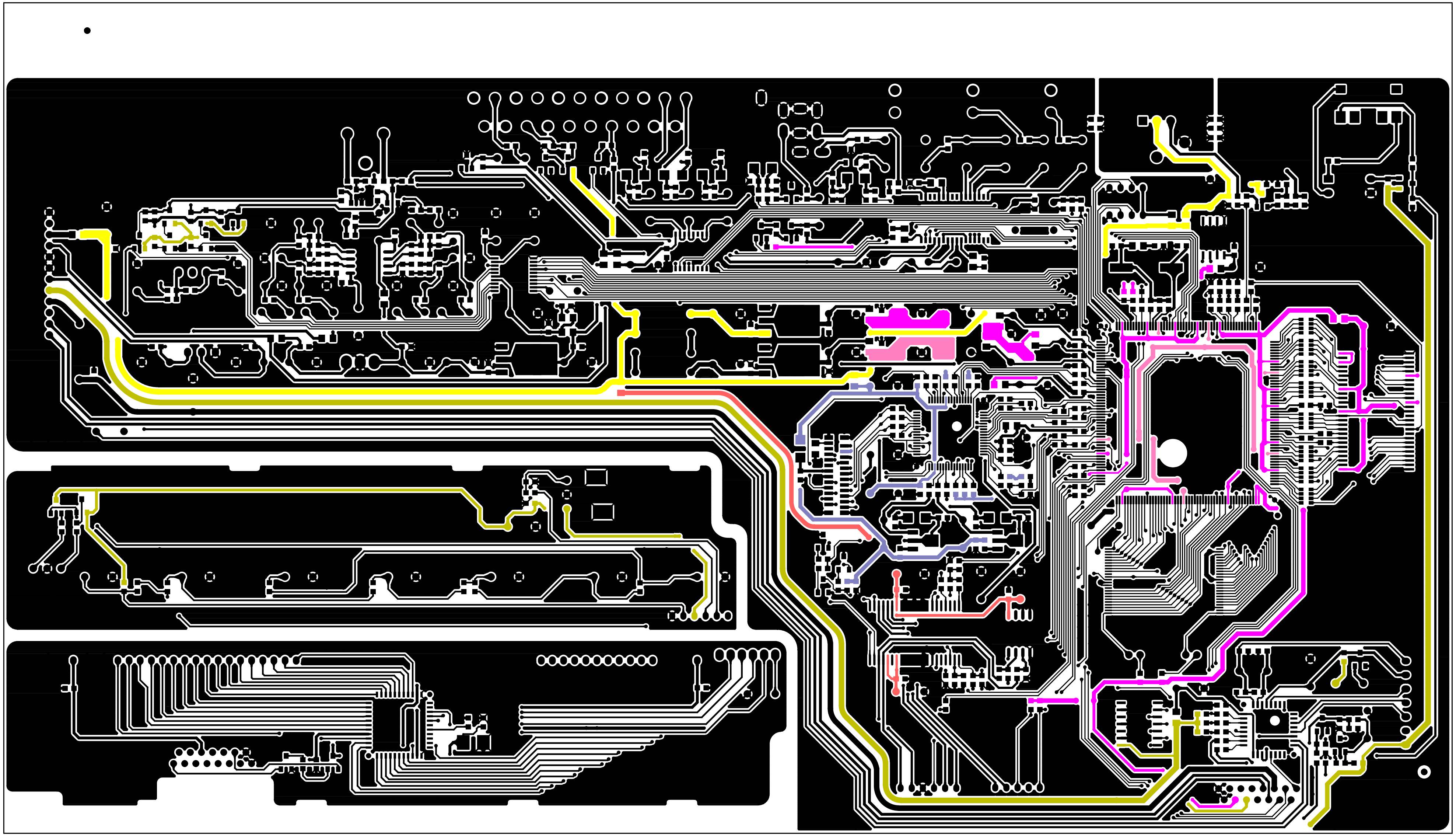


DVD 27-50629.pcb - Mon Dec 26 16:48:59 2005

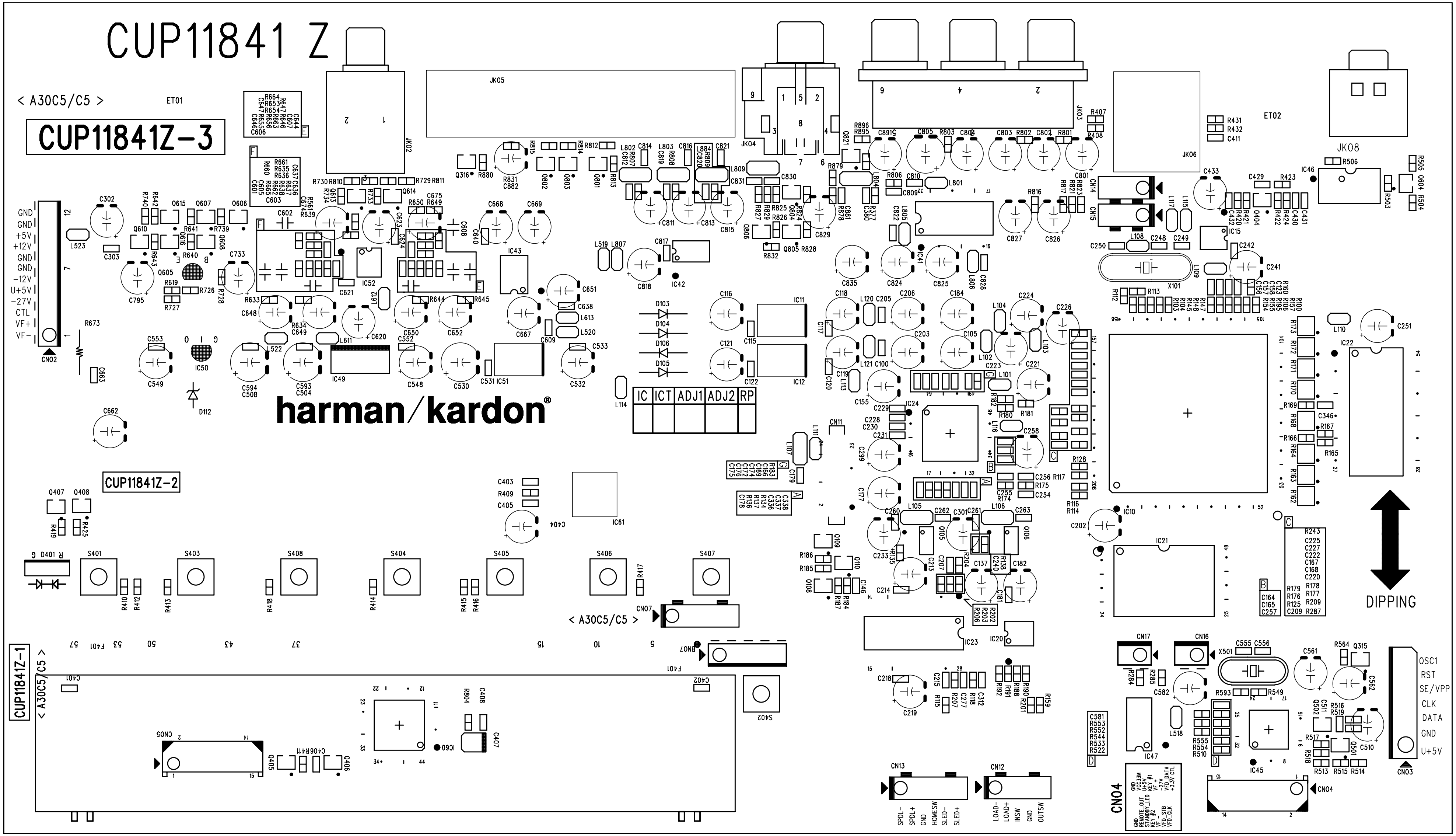

< A30C5/C5 >
CN07
< A30C5/C5 >
BN07
CN05
< A30C5/C5 >



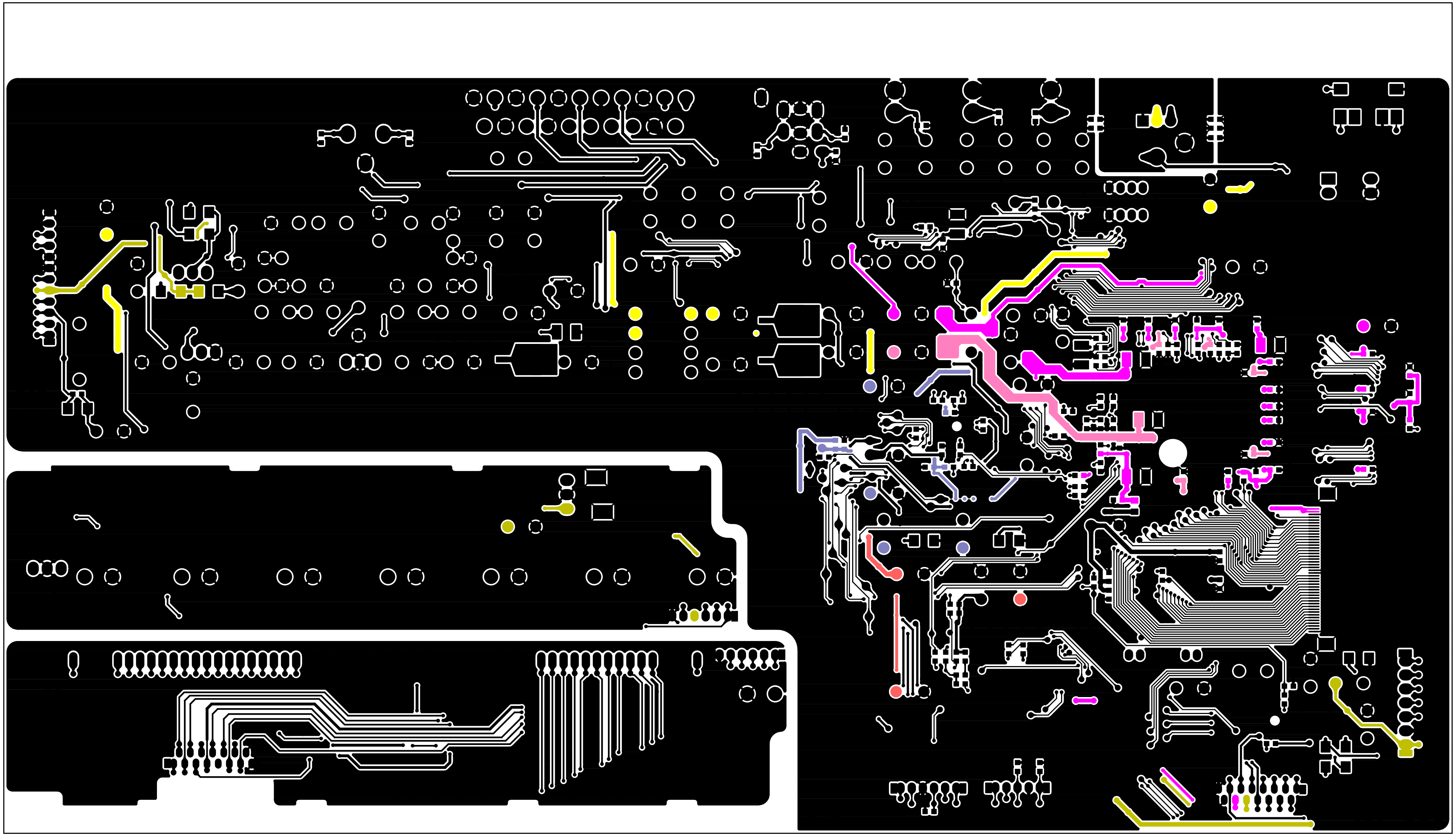
CUP11841Z MP(0722).pcb - Mon Dec 26 10:32:48 2005



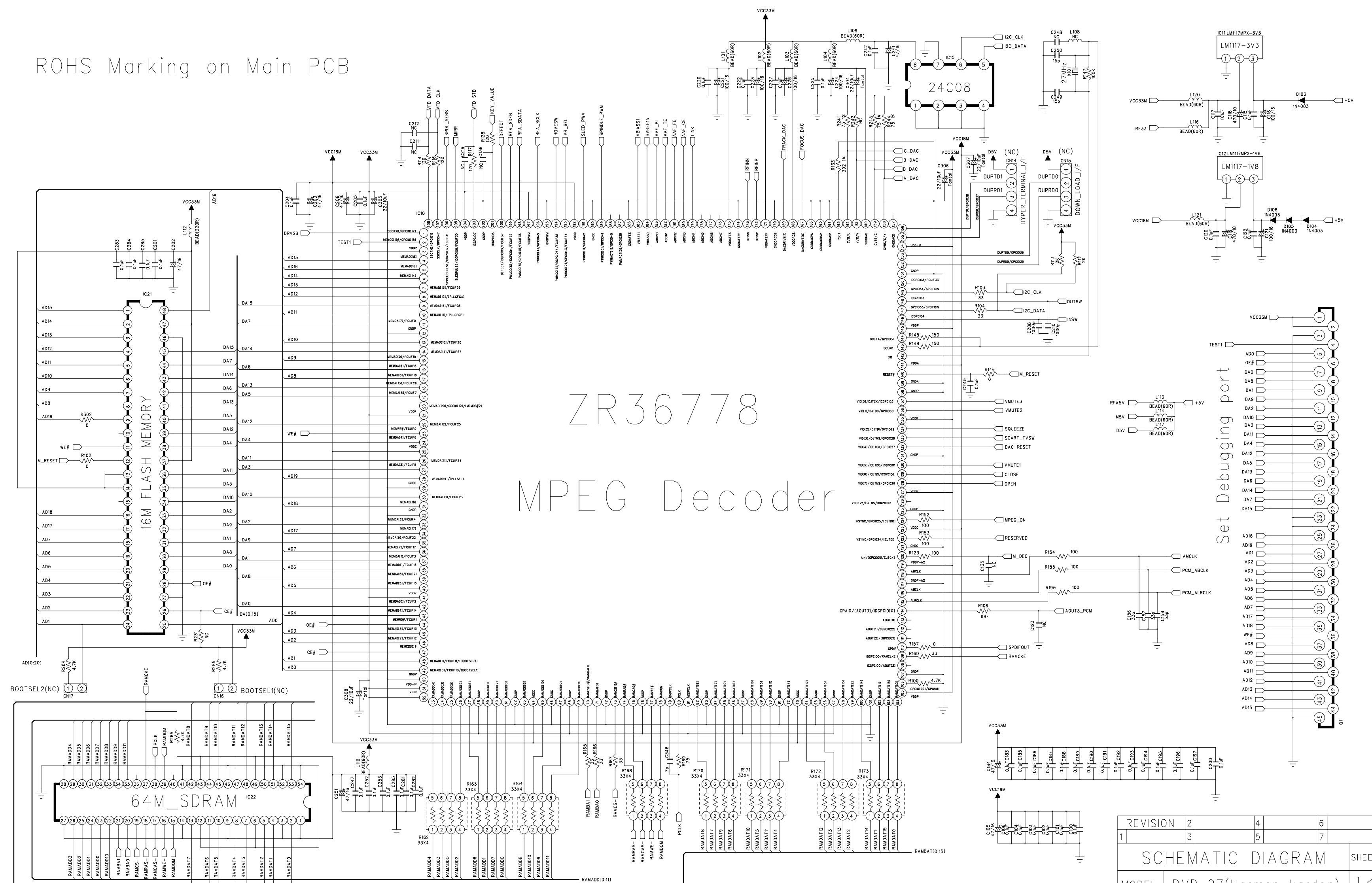
CUP11841Z MP(0722).pcb - Mon Dec 26 10:25:43 2005



CUP11841Z MP(0722).pcb - Mon Dec 26 10:30:56 2005

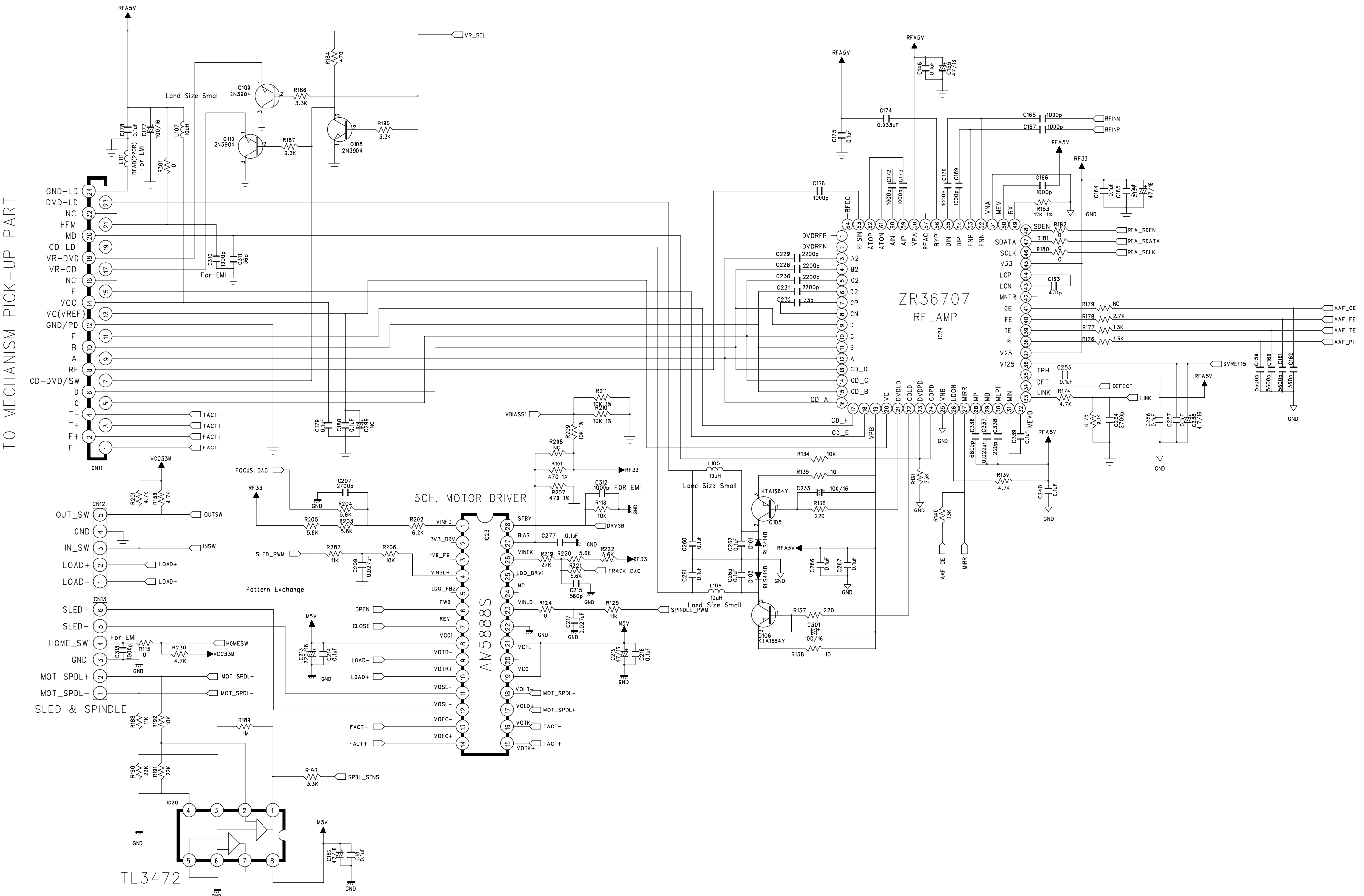


CUP11841Z MP(0722).pcb - Mon Dec 26 10:29:54 2005



REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	DVD 27(Harman-kardon)		1/4
DESIGN	CHECK	APPROVE	DRAWING NO
S.H. LEE	J.H. PARK	H.W. LEE	MPEG PART 1/4
05.07.25	05.07.25	05.07.25	

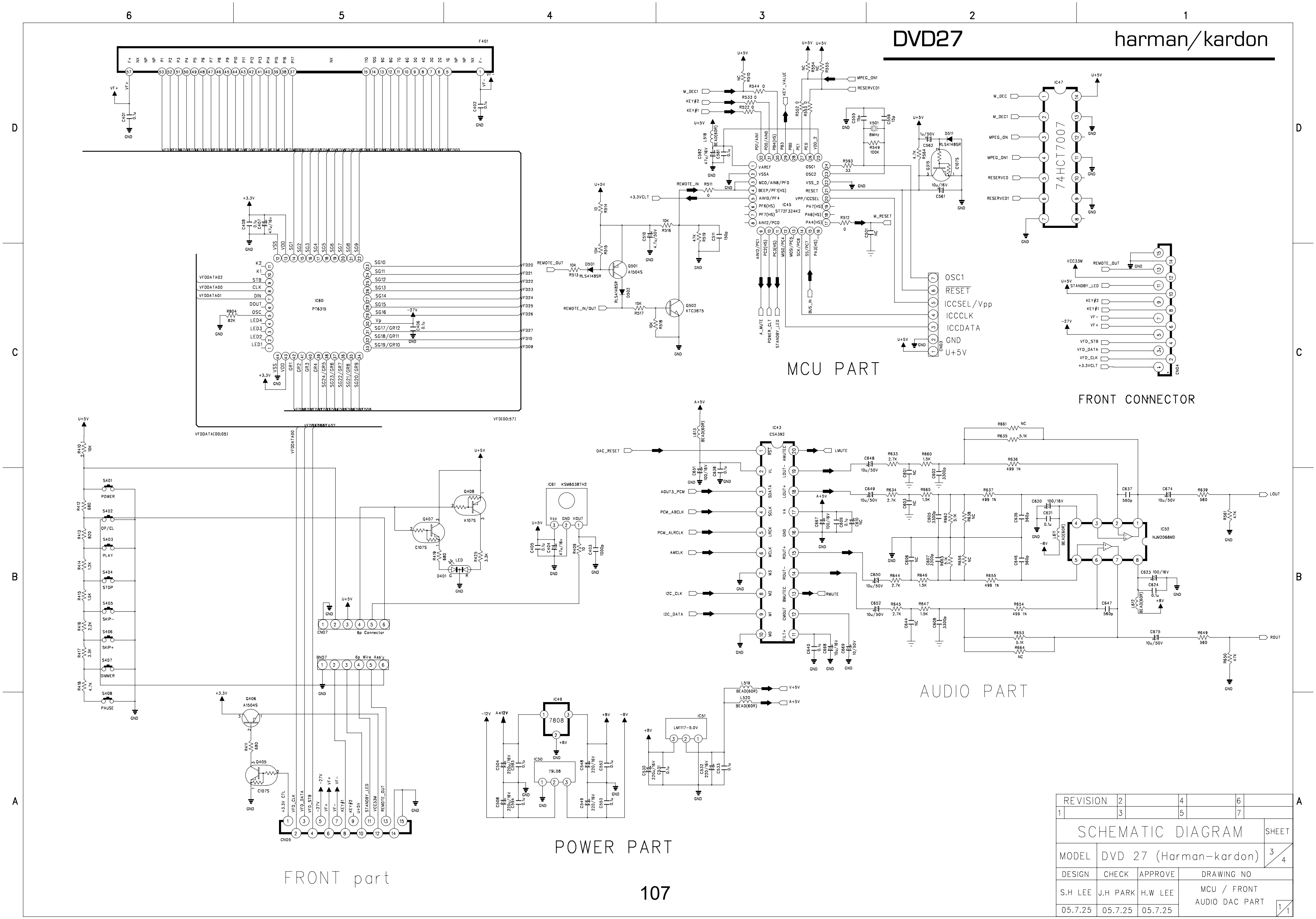


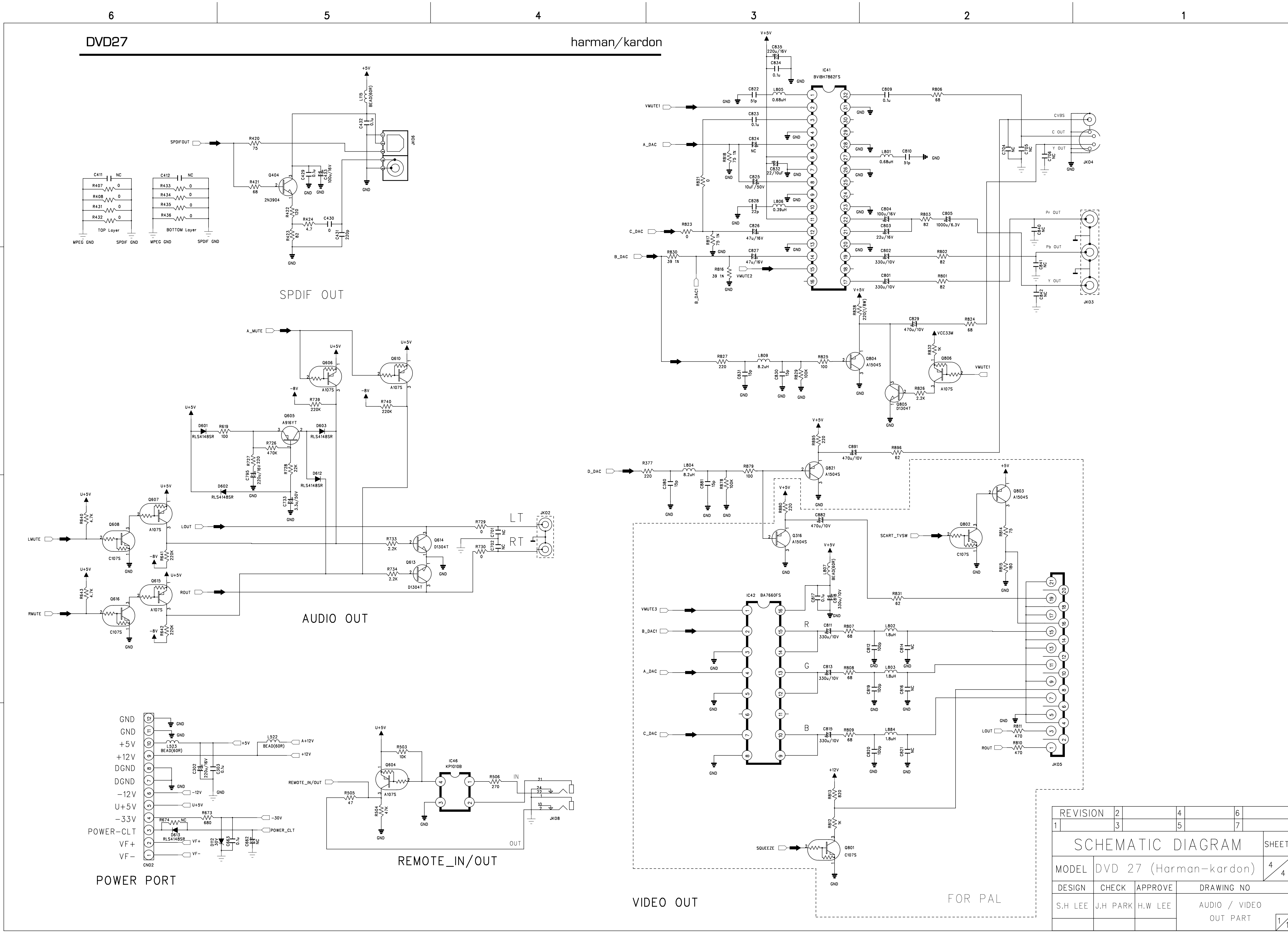
REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 2/4

MODEL: DVD 27 (Harman-kardon)

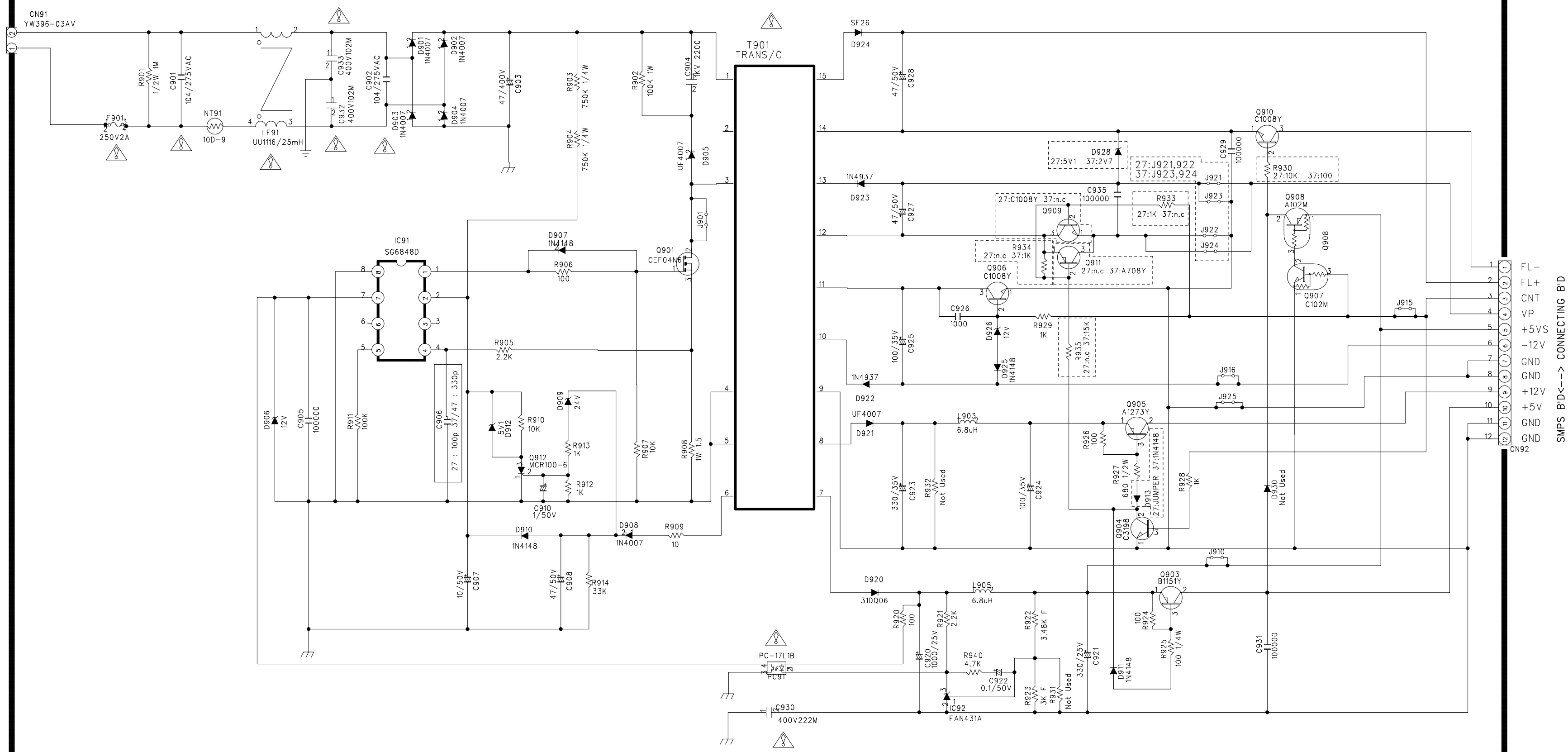
DESIGN	CHECK	APPROVE	DRAWING NO
S.H. LEE	J.H PARK	H.W LEE	SERVO PART 1/1
05.7.25	05.7.25	05.7.25	


DVD27
harman/kardon
MCU PART
FRONT CONNECTOR
AUDIO PART
POWER PART
FRONT part
IC60 PT6315
IC45 ST72F324K2
IC47 74HCT7007
IC43 CS4392
IC52 NJM2068MD
IC61 KSM603BTH2
IC49 7808
IC50 79L08
IC51 LM1117-5.0V
REVISION 1 2 3 4 5 6 7
SCHEMATIC DIAGRAM
SHEET 3/4
MODEL DVD 27 (Harman-kardon)
DESIGN S.H LEE 05.7.25
CHECK J.H PARK 05.7.25
APPROVE H.W LEE 05.7.25
DRAWING NO MCU / FRONT AUDIO DAC PART
1/1


DVD27
harman/kardon
SPDIF OUT
AUDIO OUT
POWER PORT
REMOTE_IN/OUT
VIDEO OUT
FOR PAL
SPDIFOUT
A_MUTE
LMUTE
RMUTE
LOUT
ROUT
LT
RT
JK02
JK06
JK03
JK04
JK05
JK08
CN02
IC41
BV8H7862FS
IC42
BA7660FS
IC46
KP1010B
VMUTE1
VMUTE2
VMUTE3
A_DAC
B_DAC
C_DAC
D_DAC
B_DAC1
CVBS
C OUT
Y OUT
Pr OUT
Pb OUT
SCART_TVSW
SQUEEZE
REMOTE_IN/OUT
IN
OUT
GND
GND
+5V
+12V
DGND
DGND
-12V
U+5V
-33V
POWER-CLT
VF+
VF-
TOP Layer
BOTTOM Layer
MPEG GND
SPDIF GND
R
G
B
REVISION
SCHEMATIC DIAGRAM
SHEET
4/4
MODEL
DVD 27 (Harman-kardon)
DESIGN
CHECK
APPROVE
DRAWING NO
S.H LEE
J.H PARK
H.W LEE
AUDIO / VIDEO OUT PART
1/1

DVD27

harman/kardon



DVD 27
D913 : JUMPER R935 : N.C R934 : N.C
Q909 : C1008Y R933 : 1K Q911 : N.C
D928 : 5V1 R930 : 10K J923, J924 : N.C
J921, J922 : CONNECTION C906 : 100p

DVD 37/47
D913 : 1N4148 R935 : 15K R934 : 1K
Q911 A708Y Q909 : N.C R933 : N.C
D928 : 2V7 R930 : 100 C906 : 330p
J921, J922 : N.C J923, J924 : CONNECTION

**IMPORTANT SAFETY NOTICE.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS.
USE ONLY MANUFACTUREY'S SPECIFIED PARTS.

**THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM

**THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
1pF = 10^{-6} uF

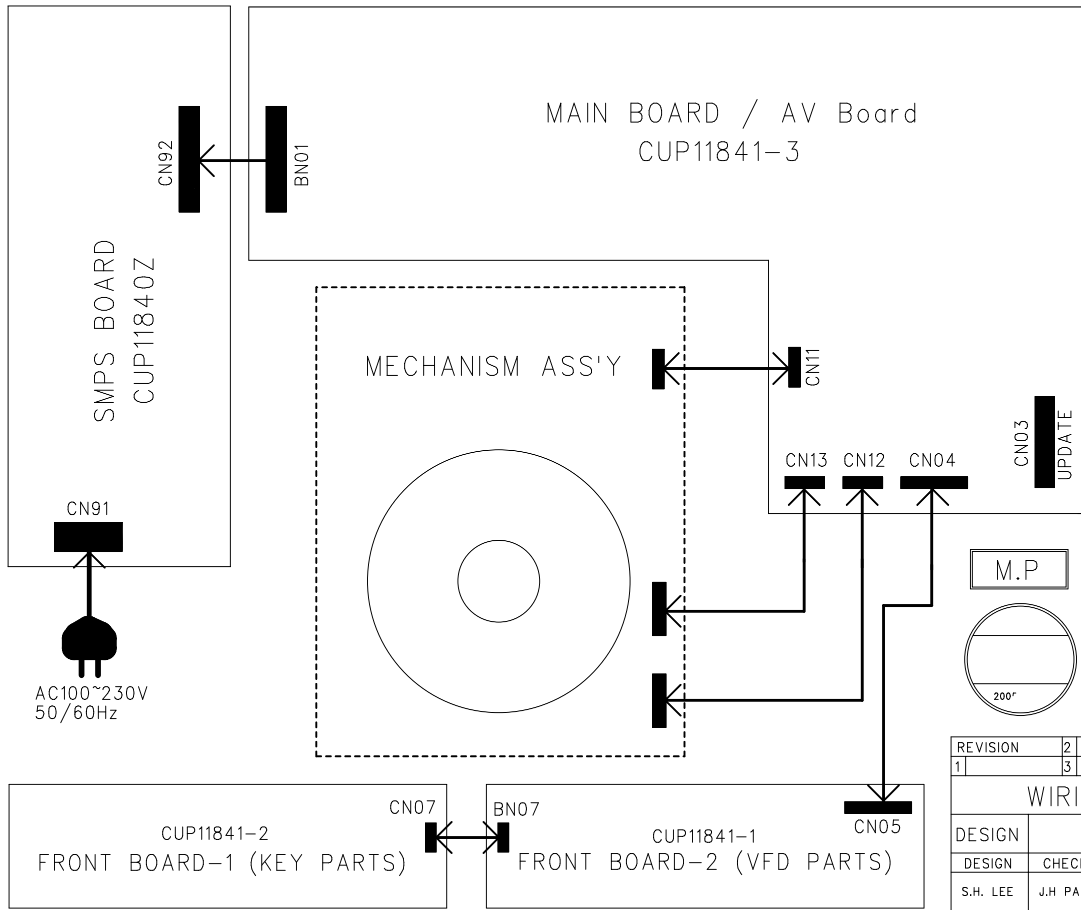
**THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANYTIME
WITH THE IMPROVEMENT OF PERFORMANCE

2005.11.23

MP

REVISION	2		4		6
1	3		5		7

SCHEMATIC DIAGRAM			SHEET
MODEL	DVD 27/37/47		
DESIGN	CHECK	APPROVE	DRAWING NO
S.H.Lee	J.H.PARK	H.W.Lee	1840SCMZ
05.11.23	05.11.23	05.11.23	(SMPS) 1/1



PIN DISCRIPTION

CN92<--->BN01

1	VF(-)
2	VF(+)
3	PWR_CTL
4	Vp
5	U+5V
6	-12V
7	GND
8	GND
9	+12V
10	VCC(+5V)
11	GND
12	GND

CN11

1	F-
2	F+
3	T+
4	T-
5	C
6	D
7	CD-DVD/SW
8	RF
9	A
10	B
11	F
12	GND/PD
13	VC(VREF)
14	VCC
15	E
16	NC
17	VR-CD
18	VR-DVD
19	CD-LD
20	MD
21	HFM
22	NC
23	DVD-LD
24	GND-LD

CN04<--->CN05

1	+3.3V CTL
2	VFD_CLK
3	VFD_DATA
4	VFD_STB
5	Vp(-27V)
6	VF+
7	VF-
8	KEY#1
9	KEY#2
10	U+5V
11	STANDBY LED
12	VCC33M
13	REMOTE OUT
14	GND
15	GND

CN12

1	LOAD-
2	LOAD+
3	IN SW
4	GND
5	OUT SW

CN03

1	U+5V
2	GND
3	DATA
4	CLK
5	SE/VPP
6	RST
7	OSC1

CN13

1	SPDL-
2	SPDL+
3	GND
4	HOME SW
5	SLED-
6	SLED+

REVISION	2	4	6
1	3	5	7

WIRING DIAGRAM			SHEET
DESIGN	DVD 27		
DESIGN	CHECK	APPROVE	
S.H. LEE	J.H PARK	H.W LEE	11841WCMZ
2005.11.01	2005.11.01	2005.11.01	